



## 9.5.9.2 Host Wake Up Control Status Register Descriptions

**Note:** All Wake-Up registers (Pg. 800-801) are not cleared when PHY reset is asserted. These registers are only cleared when internal power on reset is de-asserted or when cleared by the software device driver.

### 9.5.9.2.1 Receive Control – RCTL PHY Address 01, Page 800, Register 0

Field Name	Bit(s)	Type	Default	Description
UPE	0	RW	0b	Unicast Promiscuous Enable (UPE): 0b = Disabled 1b = Enabled
MPE	1	RW	0b	Multicast Promiscuous Enable (MPE): 0b = Disabled. 1b = Enabled.
SAE	2	RW	1b	Slave Access Enable (SAE): 0b = Access disabled, the filters are active. 1b = Access enabled, the filters are not active.
MO	4:3	RW	00b	Multicast Offset (MO) This determines which bits of the incoming multicast address are used in looking up the bit vector. 00b = [47:38] 01b = [46:37] 10b = [45:36] 11b = [43:34]
BAM	5	RW	0b	Broadcast Accept Mode (BAM): 0b = Ignore broadcast (unless it matches through exact or imperfect filters) 1b = Accept broadcast packets.
PMCF <sup>1</sup>	6	RW	0b	Pass MAC Control Frames (PMCF) 0b = Do not (specially) pass iMAC control frames. 1b = Pass any iMAC control frame (type field value of 0x8808).
RFCE	7	RW	0b	Receive Flow Control Enable (RFCE) Indicates that the I219 responds to the reception of flow control packets. If auto-negotiation is enabled, this bit is set to the negotiated duplex value.
Reserved	15:8	RO	0x00	Reserved.

1. PMCF controls the usage of MAC control frames (including flow control). A MAC control frame in this context must be addressed to the flow control multicast address 0x0100\_00C2\_8001 and match the type field (0x8808). If PMCF=1b, then frames meeting this criteria participate in wake up filtering.



### 9.5.9.2.2 Wake Up Control – WUC PHY Address 01, Page 800, Register 1

Field Name	Bit(s)	Type	Default	Description
APME	0	RW/SN		Advance Power Management Enable (APME) If set to 1b, APM wake up is enabled.
PME_En	1	RW/V		PME_En If set to 1b, ACPI wake up is enabled.
PME_Status	2	RWC		PME_Status This bit is set when the I219 receives a wake up event. This bit is cleared by writing 1b to clear or by clearing the Host_WU_Active/ME_WU_Active bits.
LSCED	3	RW	0b	Link Status Change on Energy Detect (LSCED) When this bit set enable wake in energy on the lines (instead of actual link status change). By default this bit is set to 0b.
LSCWE	4	RW/SN	0b	Link Status Change Wake Enable (LSCWE) Enables wake on link status change as part of APM wake capabilities.
LSCWO	5	RW/SN	0b	Link Status Change Wake Override (LSCWO) If set to 1b, wake on link status change does not depend on the LNK bit in the WUFC register. Instead, it is determined by the APM settings in the WUC register.
Reserved	13:6	RO	0x00	Reserved.
FLX6	14	RW	0b	Flexible filter 6 enable.
FLX7	15	RW	0b	Flexible filter 7 enable

### 9.5.9.2.3 Wake Up Filter Control – WUFC PHY Address 01, Page 800, Register 2

This register is used to enable each of the pre-defined and flexible filters for wake up support. A value of 1b means the filter is turned on, and a value of 0b means the filter is turned off.

Field Name	Bit(s)	Type	Default	Description
LNKC	0	RW	0b	Link status change wake up enable.
MAG	1	RW	0b	Magic packet wake up enable.
EX	2	RW	0b	Directed exact wake up enable.
MC	3	RW	0b	Directed multicast wake up enable.
BC	4	RW	0b	Broadcast wake up enable.
ARP	5	RW	0b	ARP/IPv4 request packet wake up enable. IPv4 filtering applies only to the 3 host IPv4 addresses in IP4AT.



Field Name	Bit(s)	Type	Default	Description
IPV4	6	RW	0b	Directed IPv4 packet wake up enable. IPv4 filtering applies only to the 3 host IPv4 addresses in IP4AT.
IPV6	7	RW	0b	Directed IPv6 packet wake up enable.
Reserved	8	RO	0b	Reserved.
FLX4	9	RW	0b	Flexible filter 4 enable.
FLX5	10	RW	0b	Flexible filter 5 enable.
NoTCO	11	RW	0b	Ignore TCO packets for host wake up. If the NoTCO bit is set, then any packet that passes the manageability packet filtering does not cause a host wake up event even if it passes one of the host wake up filters.
FLX0	12	RW	0b	Flexible filter 0 enable.
FLX1	13	RW	0b	Flexible filter 1 enable.
FLX2	14	RW	0b	Flexible filter 2 enable.
FLX3	15	RW	0b	Flexible filter 3 enable.

#### 9.5.9.2.4 Wake Up Status – WUS PHY Address 01, Page 800, Register 3

This register is used to record statistics about all wake up packets received. Note that packets that match multiple criteria might set multiple bits. Writing a 1b to any bit clears that bit.

This register is not cleared when PHY reset is asserted. It is only cleared when internal power on reset is de-asserted or when cleared by the software device driver.

Field Name	Bit(s)	Type	Default	Description
LNKC	0	RWC	0b	Link status changed.
MAG	1	RWC	0b	Magic packet received.
EX	2	RWC	0b	Directed exact packet received. The packet's address matched one of the 7 pre-programmed exact values in the Receive Address registers.
MC	3	RWC	0b	Directed multicast packet received. The packet was a multicast packet that was hashed to a value that corresponded to a 1-bit in the multicast table array.
BC	4	RWC	0b	Broadcast packet received.
ARP	5	RWC	0b	ARP/IPv4 request packet received.
IPV4	6	RWC	0b	Directed IPv4 packet received.
IPV6	7	RWC	0b	Directed IPv6 packet received.



Field Name	Bit(s)	Type	Default	Description
FLX4	8	RWC	0b	Flexible filter 4 match.
FLX5	9	RWC	0b	Flexible filter 5 match.
FLX6	10	RWC	0b	Flexible filter 6 match.
FLX7	11	RWC	0b	Flexible filter 7 match.
FLX0	12	RWC	0b	Flexible filter 0 match.
FLX1	13	RWC	0b	Flexible filter 1 match.
FLX2	14	RWC	0b	Flexible filter 2 match.
FLX3	15	RWC	0b	Flexible filter 3 match.

#### 9.5.9.2.5 Receive Address Low – RAL PHY Address 01, Page 800, Registers 16-17

Field Name	Bit(s)	Type	Default	Description
RAL	31:0	RW	0	Receive Address Low (RAL) The lower 32 bits of the 48-bit Ethernet address.

#### 9.5.9.2.6 Receive Address High – RAH PHY Address 01, Page 800, Registers 18-19

Field Name	Bit(s)	Type	Default	Description
RAH	15:0	RW	X	Receive Address High (RAH) The upper 16 bits of the 48-bit Ethernet address.
Reserved	17:16	RW	0x0	Reserved.
Reserved	30:18	RO	0x00	Reserved. Reads as 0b and is ignored on writes.
AV	31	RW	0b	Address valid (AV) When this bit is set, the relevant RAL and RAH are valid (compared against the incoming packet).

#### 9.5.9.2.7 Shared Receive Address Low – SHRAL PHY Address 01, Page 800, Registers 20-21 + 4\*n (n=0...10)

Field Name	Bit(s)	Type	Default	Description
RAL	31:0	RW	X	Receive Address Low (RAL) The lower 32 bits of the 48-bit Ethernet address n (n=0...10).





### 9.5.9.2.8 Shared Receive Address High – SHRAH PHY Address 01, Page 800, Registers 22-23 + 4\*n (n=0...8,10)

Field Name	Bit(s)	Type	Default	Description
RAH	15:0	RW	X	Receive Address High (RAH) The upper 16 bits of the 48-bit Ethernet address n (n=0...8,10).
Reserved	17:16	RW	0x0	Reserved.
Reserved	30:18	RO	0x00	Reserved. Reads as 0b and is ignored on writes.
AV	31	RW	0b	Address valid (AV) When this bit is set, the relevant RAL and RAH are valid (compared against the incoming packet).

### 9.5.9.2.9 Shared Receive Address High 9 – SHRAH[9] PHY Address 01, Page 800, Registers 58-59

Field Name	Bit(s)	Type	Default	Description
RAH	15:0	RW	X	Receive Address High (RAH) The upper 16 bits of the 48-bit Ethernet address 9.
Reserved	17:16	RW	0x0	Reserved.
Reserved	29:18	RO	0x00	Reserved. Reads as 0x00 and is ignored on writes.
MAV	30	RW	0b	All Nodes Multicast Address valid (MAV) The all nodes multicast address (33:33:00:00:00:01) is valid when this bit is set. Note that 0x33 is the first byte on the wire.
AV	31	RW	0b	Address valid (AV) When this bit is set, the relevant address 3 is valid (compared against the incoming packet).

### 9.5.9.2.10 IP Address Valid – IPAV PHY Address 01, Page 800, Register 64

Field Name	Bit(s)	Type	Default	Description
Reserved	0	RO	0b	Reserved.
IP4AT1 address valid	1	RW	0b	IPv4 address 1 valid.
IP4AT2 address valid	2	RW	0b	IPv4 address 2 valid.
IP4AT3 address valid	3	RW	0b	IPv4 address 3 valid.
IP6AT3 address valid	4	RW	0b	IPv6 address 3 valid.



Field Name	Bit(s)	Type	Default	Description
IP6AT2 address valid	5	RW	0b	IPv6 address 2 valid.
IP6AT1 address valid	6	RW	0b	IPv6 address 1 valid.
IP6AT0 address valid	7	RW	0b	IPv6 address 0 valid (Duplicate of bit 15).
	8	RW	0b	Enable L2 for IPv6 multicast according to IP6AT0.
	9	RW	0b	Enable L2 for IPv6 multicast according to IP6AT1
	10	RW	0b	Enable L2 for IPv6 multicast according to IP6AT2
	11	RW	0b	Enable L2 for IPv6 multicast according to IP6AT3
Reserved	14:12	RO	0x0	Reserved.
	15	RW	0b	V60 IPv6 address valid.

The IP address valid indicates whether the IP addresses in the IP address table are valid.

#### 9.5.9.2.11 Proxy Control – PRXC PHY Address 01, Page 800, Register 70

Field Name	Bit(s)	Type	Default	Description
Proxy_mode	0	RW	0b	Should be set in the end of Proxy configuration. That's the last MDIO access to PHY, unless we put arbitration on MDIO accesses between Proxy uCtl and regular MDIO accesses through MAC). As long as this bit is clear, Proxy logic is under reset.
Code_loaded	1	RW	0b	Set either by software after loading the uCode through MDIO, or by hardware after reception of the Code packet from MAC (the first packet after setting PRXC.Nxt_pkt_is_code).
Code_from_MDIO	2	RW	0b	Should be set by software before it starts loading the instruction code memory through MDIO accesses to page 802.
Nxt_pkt_is_code	3	RW	0b	Should be set by software before it transmits uCode packet.
	4	RW	0b	Auto disable proxying after link-down deactivation period.
ARP PProxy Enable	5	RW	0b	ARP PProxy Enable.
ND Proxy Enable	6	RW	0b	ND Proxy Enable.
Reserved	7	RW	0b	Reserved.
	13:8	RW	0b	Link Down deactivation period in 1 seconds granularity.
Reserved	14	RW	0b	Reserved.
Ready_for_Code	15	RW	0b	This bit is set by HW post setting of Code_from_MDIO or Nxt_pkt_is_code indicating software is ready for the code load.



### 9.5.9.2.12 Proxy Code Checksum – PRCC PHY Address 01, Page 800, Register 71

Field Name	Bit(s)	Type	Default	Description
Proxy Code Checksum	15:0	RO	0x0000	This register holds the checksum calculation for the proxy code loaded to the transmit FIFO as a packet starting from the start of frame till the end of frame.

### 9.5.9.2.13 Proxy Control 2 – PRXC2 PHY Address 01, Page 800, Register 72

Field Name	Bit(s)	Type	Default	Description
Reserved	13:0	RO	0b	Reserved.
MLD Proxy Enable	14	RW	0b	MLD Proxy Enable
Reserved	15	RO	0b	Reserved.

### 9.5.9.2.14 Flex Filters Proxy Control – FFPRXC PHY Address 01, Page 800, Register 75

Field Name	Bit(s)	Type	Default	Description
	0	RW	0b	Route Flex filter 0 to the proxy uController.
	1	RW	0b	Route Flex filter 1 to the proxy uController.
	2	RW	0b	Route Flex filter 2 to the proxy uController.
	3	RW	0b	Route Flex filter 3 to the proxy uController.
	4	RW	0b	Route Flex filter 4 to the proxy uController.
	5	RW	0b	Route Flex filter 5 to the proxy uController.
	6	RW	0b	Route Flex filter 6 to the proxy uController.
	7	RW	0b	Route Flex filter 7 to the proxy uController.
Flex Filter Match Status	15:8	RWC	0x00	An incoming packet matching one of the flex filters will set a bit in this status. The bits are cleared on write of 1. Bit 8 = Flex filter 0 match Bit 9 = Flex filter 1 match Bit 10 = Flex filter 2 match Bit 11 = Flex filter 3 match Bit 12 = Flex filter 4 match Bit 13 = Flex filter 5 match Bit 14 = Flex filter 6 match Bit 15 = Flex filter 7 match



### 9.5.9.2.15 Wake Up Filter Control 2 – WUFC2 PHY Address 01, Page 800, Register 76

Field Name	Bit(s)	Type	Default	Description
FLX8	0	RW	0b	Flexible filter 8 enable.
FLX9	1	RW	0b	Flexible filter 9 enable.
FLX10	2	RW	0b	Flexible filter 10 enable.
FLX11	3	RW	0b	Flexible filter 11 enable.
FLX12	4	RW	0b	Flexible filter 12 enable.
FLX13	5	RW	0b	Flexible filter 13 enable.
FLX14	6	RW	0b	Flexible filter 14 enable.
FLX15	7	RW	0b	Flexible filter 15 enable.
Reserved	15:8	RO	0x00	Reserved.

### 9.5.9.2.16 Wake Up Filter Status 2 – WUS2 PHY Address 01, Page 800, Register 77

Field Name	Bit(s)	Type	Default	Description
FLX8	0	RW	0b	Flexible filter 8 matched.
FLX9	1	RW	0b	Flexible filter 9 matched.
FLX10	2	RW	0b	Flexible filter 10 matched.
FLX11	3	RW	0b	Flexible filter 11 matched.
FLX12	4	RW	0b	Flexible filter 12 matched.
FLX13	5	RW	0b	Flexible filter 13 matched.
FLX14	6	RW	0b	Flexible filter 14 matched.
FLX15	7	RW	0b	Flexible filter 15 matched.
Reserved	15:8	RO	0x00	Reserved.

### 9.5.9.2.17 Wake Up Filter Control 3 – WUFC3 PHY Address 01, Page 800, Register 78

Content TBD



### 9.5.9.2.18 Wake Up Filter Status 3 – WUS3 PHY Address 01, Page 800, Register 79

Content TBD

### 9.5.9.2.19 Wake Up Filter Control 4 – WUFC4 PHY Address 01, Page 800, Register 80

Content TBD

### 9.5.9.2.20 Wake Up Filter Status 4 – WUS4 PHY Address 01, Page 800, Register 81

Content TBD

### 9.5.9.2.21 IPv4 Address Table – IP4AT PHY Address 01, Page 800, Registers 82-83 + 2\*n (n=0, 1, 2)

Field Name	Bit(s)	Type	Default	Description
IPADD	31:0	RW	X	IP address n (n= 0, 1, 2).

**Note:** The IPv4 address table is used to store the three IPv4 addresses for ARP/IPv4 request packets and directed IPv4 packet wake ups.

### 9.5.9.2.22 IPv6 Address Table – IP6AT[3:0] PHY Address 01, Page 800, Registers 88-89 + 2\*n (n=0...3)

The IPv6 address table is used to store the IPv6 addresses for directed IPv6 packet wake up (only using the first IPv6 address) and network proxy filtering.

Field Name	Bit(s)	Type	Default	Description
IPv6 Address	31:0	RW	0x0	IPv6 address bytes n*4...n*4+3 (n=0, 1, 2, 3) while byte 0 is first on the wire and byte 15 is last.

Configuration example for IPv6 address: fe80:0:0:0:200:1ff:fe30:100

```
01.800.88 - 0x80fe
01.800.89 - 0x0000
01.800.90 - 0x0000
01.800.91 - 0x0000
01.800.92 - 0x0002
01.800.93 - 0xff01
01.800.94 - 0x30fe
01.800.95 - 0x0001
```



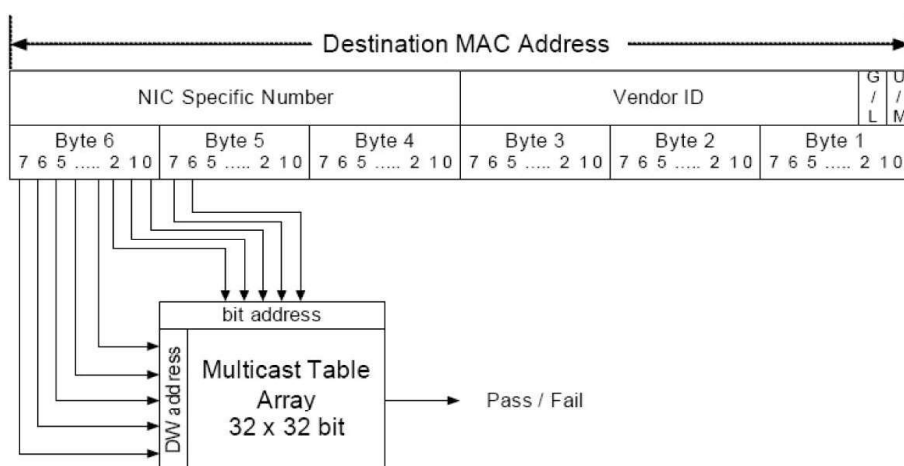
### 9.5.9.2.23 Multicast Table Array – MTA[31:0] PHY Address 01, Page 800, Registers 128-191

Field Name	Bit(s)	Type	Default	Description
Bit Vector	RW	31:0	X	Word-wide bit vector specifying 32 bits in the multicast address filter table.

There is one register per 32 bits of the multicast address table for a total of 32 registers (thus the MTA[31:0] designation). The size of the word array depends on the number of bits implemented in the multicast address table. Software must mask to the desired bit on reads and supply a 32-bit word on writes.

**Note:** All accesses to this table must be 32-bit.

Figure 9-1 shows the multicast lookup algorithm.



**Figure 9-1 Multicast Table Array Algorithm**

The destination address shown represents the internally stored ordering of the received destination address. Note that Byte 1 bit 0 shown in Figure 9-1 is the first on the wire. The bits that are directed to the multicast table array in this diagram match a multicast offset in the CTRL register equals 00b. The complete multicast offset options are:

Multicast Offset	Bits Directed to the Multicast Table Array
00b	DA[47:38] = Byte 6 bits 7:0, Byte 5 bits 1:0
01b	DA[46:37] = Byte 6 bits 6:0, Byte 5 bits 2:0
10b	DA[45:36] = Byte 6 bits 5:0, Byte 5 bits 3:0
11b	DA[43:34] = Byte 6 bits 3:0, Byte 5 bits 5:0



#### 9.5.9.2.24 Flexible Filter Value Table LSB – FFVT\_01 PHY Address 01, Page 800, Registers 256 + 2\*n (n=0...127)

Field Name	Bit(s)	Type	Default	Description
Value 0	RW	7:0	X	Value of filter 0 byte n (n=0, 1... 127).
Value 1	RW	15:0	X	Value of filter 1 byte n (n=0, 1... 127).

There are 128 filter values. The flexible filter value is used to store the one value for each byte location in a packet for each flexible filter. If the corresponding mask bit is one, then the flexible filter compares the incoming data byte to the values stored in this table.

In the I219 since each address contains 16 bits, only the least significant bytes are stored in those addresses.

#### 9.5.9.2.25 Flexible Filter Value Table MSBs – FFVT\_23 PHY Address 01, Page 800, Registers 257 + 2\*n (n=0...127)

Field Name	Bit(s)	Type	Default	Description
Value 2	7:0	RW	X	Value of filter 2 byte n (n=0, 1... 127).
Value 3	15:8	RW	X	Value of filter 3 byte n (n=0, 1... 127).

There are 128 filter values. The flexible filter value is used to store the one value for each byte location in a packet for each flexible filter. If the corresponding mask bit is one, then the flexible filter compares the incoming data byte to the values stored in this table.

In the I219 since each address contains 16 bits, only the most significant bytes are stored in those addresses.

**Note:** Before writing to the flexible filter value table the software device driver must first disable the flexible filters by writing zeros to the Flexible Filter Enable bits of the WUFC register (WUFC.FLXn).

#### 9.5.9.2.26 Flexible Filter Value Table – FFVT\_45 PHY Address 01, Page 800, Registers 512 + 2\*n (n=0...127)

Field Name	Bit(s)	Type	Default	Description
Value 4	7:0	RW	X	Value of filter 4 byte n (n=0, 1... 127).
Value 5	15:8	RW	X	Value of filter 5 byte n (n=0, 1... 127).



### 9.5.9.2.27 Flexible Filter Value Table – FFVT\_67 PHY Address 01, Page 800, Registers 1024 + 2\*n (n=0...127)

Field Name	Bit(s)	Type	Default	Description
Value 6	7:0	RW	X	Value of filter 6 byte n (n=0, 1... 127).
Value 7	15:8	RW	X	Value of filter 7 byte n (n=0, 1... 127).

### 9.5.9.2.28 Flexible Filter Mask Table – FFMT PHY Address 01, Page 800, Registers 768 + n (n=0...127)

Field Name	Bit(s)	Type	Default	Description
Mask 0	0	RW	X	Mask for filter 0 byte n (n=0, 1... 127).
Mask 1	1	RW	X	Mask for filter 1 byte n (n=0, 1... 127).
Mask 2	2	RW	X	Mask for filter 2 byte n (n=0, 1... 127).
Mask 3	3	RW	X	Mask for filter 3 byte n (n=0, 1... 127).
Mask 4	4	RW	X	Mask for filter 4 byte n (n=0, 1... 127).
Mask 5	5	RW	X	Mask for filter 5 byte n (n=0, 1... 127).
Mask 6	6	RW	X	Mask for filter 6 byte n (n=0, 1... 127).
Mask 7	7	RW	X	Mask for filter 7 byte n (n=0, 1... 127).
Reserved	15:8	RO	X	Reserved.

There are 128 mask entries. The flexible filter mask and table is used to store the four 1-bit masks for each of the first 128 data bytes in a packet, one for each flexible filter. If the mask bit is one, the corresponding flexible filter compares the incoming data byte at the index of the mask bit to the data byte stored in the flexible filter value table.

**Note:** Before writing to the flexible filter mask table the software device driver must first disable the flexible filters by writing zeros to the Flexible Filter Enable bits of the WUFC register (WUFC.FLXn).





### 9.5.9.2.29 Flexible Filter Length Table – FFLT03 PHY Address 01, Page 800, Registers 896 + n (n=0...3)

Field Name	Bit(s)	Type	Default	Description
LEN	10:0	RW	X	Minimum length for flexible filter n (n=0, 1... 3).
Reserved	RO	15:11	X	Reserved.

All reserved fields read as zeros and are ignored on writes.

There are eight flexible filters lengths covered by FFLT03, FFLT45, FFLT67 registers. The flexible filter length table stores the minimum packet lengths required to pass each of the flexible filters. Any packets that are shorter than the programmed length won't pass that filter. Each flexible filter considers a packet that doesn't have any mismatches up to that point to have passed the flexible filter when it reaches the required length. It does not check any bytes past that point.

**Note:** Before writing to the flexible filter length table the software device driver must first disable the flexible filters by writing zeros to the Flexible Filter Enable bits of the WUFC register (WUFC.FLXn).

### 9.5.9.2.30 Flexible Filter Length Table – FFLT45 PHY Address 01, Page 800, Registers 904 + n (n=0...1)

Field Name	Bit(s)	Type	Default	Description
LEN	10:0	RW	X	Minimum length for flexible filter n (n=0, 1).
Reserved	15:11	RO	X	Reserved.

### 9.5.9.2.31 Flexible Filter Length Table – FFLT67 PHY Address 01, Page 800, Registers 908 + n (n=0...1)

Field Name	Bit(s)	Type	Default	Description
LEN	10:0	RW	X	Minimum length for flexible filter n (n=0, 1).
Reserved	15:11	RO	X	Reserved.



#### 9.5.9.2.32 Flexible Filter Value Table 89 – FFVT\_89 PHY Address 01, Page 800, Registers 2304 + 2\*n (n=0...127)

Field Name	Bit(s)	Type	Default	Description
	7:0	RW	X	Value of filter 8 byte n (n=0, 1... 127).
	15:8	RW	X	Value of filter 9 byte n (n=0, 1... 127).

There are 128 filter values. The flexible filter value is used to store the one value for each byte location in a packet for each flexible filter. If the corresponding mask bit is one, then the flexible filter compares the incoming data byte to the values stored in this table.

#### 9.5.9.2.33 Flexible Filter Value Table 1011 – EFFVT\_1011 PHY Address 01, Page 800, Registers 2305 + 2\*n (n=0...127)

Field Name	Bit(s)	Type	Default	Description
	7:0	RW	X	Value of filter 10 byte n (n=0, 1... 127).
	15:8	RW	X	Value of filter 11 byte n (n=0, 1... 127).

There are 128 filter values. The flexible filter value is used to store the one value for each byte location in a packet for each flexible filter. If the corresponding mask bit is one, then the flexible filter compares the incoming data byte to the values stored in this table.

#### 9.5.9.2.34 Flexible Filter Value Table 1213 – FFVT\_1213 PHY Address 01, Page 800, Registers 2560 + 2\*n (n=0...127)

Field Name	Bit(s)	Type	Default	Description
	7:0	RW	X	Value of filter 12 byte n (n=0, 1... 127).
	15:8	RW	X	Value of filter 13 byte n (n=0, 1... 127).



### 9.5.9.2.35 Flexible Filter Mask Table 2 – FFMT2 PHY Address 01, Page 800, Registers 2816 + n (n=0...127)

Field Name	Bit(s)	Type	Default	Description
Mask 8	0	RW	X	Mask for filter 8 byte n (n=0, 1... 127).
Mask 9	1	RW	X	Mask for filter 9 byte n (n=0, 1... 127).
Mask 10	2	RW	X	Mask for filter 10 byte n (n=0, 1... 127).
Mask 11	3	RW	X	Mask for filter 11 byte n (n=0, 1... 127).
Mask 12	4	RW	X	Mask for filter 12 byte n (n=0, 1... 127).
Mask 13	5	RW	X	Mask for filter 13 byte n (n=0, 1... 127).
Mask 14	6	RW	X	Mask for filter 14 byte n (n=0, 1... 127).
Mask 15	7	RW	X	Mask for filter 15 byte n (n=0, 1... 127).
Reserved	15:8	RO	X	Reserved.

There are 128 mask entries. The flexible filter mask and table is used to store the four 1-bit masks for each of the first 128 data bytes in a packet, one for each flexible filter. If the mask bit is one, the corresponding flexible filter compares the incoming data byte at the index of the mask bit to the data byte stored in the flexible filter value table.

### 9.5.9.2.36 Flexible Filter Length Table 891011 – FFLT891011 PHY Address 01, Page 800, Registers 2944 + n (n=0...3)

Field Name	Bit(s)	Type	Default	Description
LEN	10:0	RW	X	Minimum length for flexible filter n (n=0, 1... 3). For filters 8, 9, 10 and 11.
Reserved	15:11	RO	X	Reserved.

### 9.5.9.2.37 Flexible Filter Length Table 1213 – FFLT1213 PHY Address 01, Page 800, Registers 2952 + n (n=0...1)

Field Name	Bit(s)	Type	Default	Description
LEN	10:0	RW	X	Minimum length for flexible filter n (n=0, 1). For filters 12 and 13.
Reserved	15:11	RO	X	Reserved.



### 9.5.9.2.38 Flexible Filter Length Table 1415 – FFLT1415 PHY Address 01, Page 800, Registers 2956 + n (n=0...1)

Field Name	Bit(s)	Type	Default	Description
LEN	10:0	RW	X	Minimum length for flexible filter n (n=0, 1). For filters 14 and 15.
Reserved	15:11	RO	X	Reserved.

### 9.5.9.2.39 Flexible Filter Value Table 1415 – FFVT\_1415 PHY Address 01, Page 800, Registers 3072 + 2\*n (n=0...127)

Field Name	Bit(s)	Type	Default	Description
	7:0	RW	X	Value of filter 14 byte n (n=0, 1... 127).
	15:8	RW	X	Value of filter 15 byte n (n=0, 1... 127).

### 9.5.9.2.40 Flexible Filter Value Table 1617 – FFVT\_1617 PHY Address 01, Page 800, Registers 4352 + 2\*n (n=0...127)

Content TBD.

### 9.5.9.2.41 Flexible Filter Value Table 1819 – FFVT\_1819 PHY Address 01, Page 800, Registers 4353 + 2\*n (n=0...127)

Content TBD.

### 9.5.9.2.42 Flexible Filter Value Table 2021 – FFVT\_2021 PHY Address 01, Page 800, Registers 4608 + 2\*n (n=0...127)

Content TBD.

### 9.5.9.2.43 Flexible Filter Value Table 2223 – FFVT\_2223 PHY Address 01, Page 800, Registers 4609 + 2\*n (n=0...127)

Content TBD.



**9.5.9.2.44 Flexible Filter Mask Table 3 – FFMT3 PHY Address 01, Page 800, Registers 4864 + n (n=0...127)**

Content TBD.

**9.5.9.2.45 Flexible Filter Length Table 1619 – FFLT1619 PHY Address 01, Page 800, Registers 4992 + n (n=0...3)**

Content TBD.

**9.5.9.2.46 Flexible Filter Length Table 2021 – FFLT2021 PHY Address 01, Page 800, Registers 5000 + n (n=0...1)**

Content TBD.

**9.5.9.2.47 Flexible Filter Length Table 2223 – FFLT2223 PHY Address 01, Page 800, Registers 5004 + n (n=0...1)**

Content TBD.

**9.5.9.2.48 Flexible Filter Value Table 2425 – FFVT\_2425 PHY Address 01, Page 800, Registers 6400 + 2\*n (n=0...127)**

Content TBD.

**9.5.9.2.49 Flexible Filter Value Table 2627 – FFVT\_2627 PHY Address 01, Page 800, Registers 6401 + 2\*n (n=0...127)**

Content TBD.

**9.5.9.2.50 Flexible Filter Value Table 2829 – FFVT\_2829 PHY Address 01, Page 800, Registers 6656 + 2\*n (n=0...127)**

Content TBD.

**9.5.9.2.51 Flexible Filter Value Table 3031 – FFVT\_3031 PHY Address 01, Page 800, Registers 6657 + 2\*n (n=0...127)**

Content TBD.



#### 9.5.9.2.52 Flexible Filter Mask Table 4 – FFMT4 PHY Address 01, Page 800, Registers 6912 + n (n=0...127)

Content TBD.

#### 9.5.9.2.53 Flexible Filter Length Table 2427 – FFLT2427 PHY Address 01, Page 800, Registers 7040 + n (n=0...3)

Content TBD.

#### 9.5.9.2.54 Flexible Filter Length Table 2829 – FFLT2829 PHY Address 01, Page 800, Registers 7048 + n (n=0...1)

Content TBD.

#### 9.5.9.2.55 Flexible Filter Length Table 3031 – FFLT3031 PHY Address 01, Page 800, Registers 7052 + n (n=0...1)

Content TBD.

#### 9.5.9.2.56 Management 2 Host Control Register – MANC2H PHY Address 01, Page 801, Registers 30-31

Field Name	Bit(s)	Type	Default	Description
FP0	0	RW	0b	Flex Port 0 (FP0) When set indicates that packets that are routed to the ME due to this filter will be sent to the HOST as well.
FP1	1	RW	0b	Flex Port 1 (FP1) When set indicates that packets that are routed to the ME due to this filter will be sent to the HOST as well.
FP2	2	RW	0b	Flex Port 2 (FP2) When set indicates that packets that are routed to the ME due to this filter will be sent to the HOST as well.
FT0	3	RW	0b	Flex TCO 0 (FT0) When set indicates that packets that are routed to the ME due to this filter will be sent to the HOST as well.
FT1	4	RW	0b	Flex TCO 1 (FT1) When set indicates that packets that are routed to the ME due to this filter will be sent to the HOST as well.
FLT_026F	5	RW	0b	026F (FLT_026F) When set indicates that packets that are routed to the ME due to this filter will be sent to the HOST as well.



Field Name	Bit(s)	Type	Default	Description
FLT_0298	6	RW	0b	0298 (FLT_0298) When set indicates that packets that are routed to the ME due to this filter will be sent to the HOST as well.
ARP_REQ	7	RW	0b	ARP_REQuest (ARP_REQ) When set indicates that packets that are routed to the ME due to this filter will be sent to the HOST as well.
ARP_RES	8	RW	0b	ARP_RESponse (ARP_RES) When set indicates that packets that are routed to the ME due to this filter will be sent to the HOST as well.
BR	9	RW	0b	Broadcast (BR) When set indicates that packets that are routed to the ME due to this filter will be sent to the HOST as well.
NE	10	RW	0b	Neighbor (NE) When set indicates that packets that are routed to the ME due to this filter will be sent to the HOST as well.
VLAN0	11	RW	0b	VLAN 0 (VLAN0) When set indicates that packets that are routed to the ME due to this filter will be sent to the HOST as well.
VLAN1	12	RW	0b	VLAN 1 (VLAN1) When set indicates that packets that are routed to the ME due to this filter will be sent to the HOST as well.
VLAN2	13	RW	0b	VLAN 2 (VLAN2) When set indicates that packets that are routed to the ME due to this filter will be sent to the HOST as well.
VLAN3	14	RW	0b	VLAN 3 (VLAN3) When set indicates that packets that are routed to the ME due to this filter will be sent to the HOST as well.
MNG_MAC	15	RW	0b	Manageability MAC (MNG_MAC) When set indicates that packets that are routed to the ME due to a match of the destination MAC address to any of the Shared Receive Addresses, are sent to the HOST as well.
FP3	16	RW	0b	Flex Port 3 (FP3) When set indicates that packets that are routed to the ME due to this filter will be sent to the HOST as well.
MNG_ANM	17	RW	0b	Manageability All Nodes Multicast MAC (MNG_ANM). When set to '1' packets that are routed to the ME due to a match of the destination MAC address to 33:33:00:00:00:01 are sent to the HOST as well.
L24IPV60	18	RW	0b	Low IPv6 address 0 (L24IPV60) When set indicates that packets that are routed to the ME due to this filter will be sent to the HOST as well.
L24IPV61	19	RW	0b	Low IPv6 address 1 (L24IPV61) When set indicates that packets that are routed to the ME due to this filter will be sent to the HOST as well.



Field Name	Bit(s)	Type	Default	Description
L24IPV62	20	RW	0b	Low IPv6 address 2 (L24IPV62) When set indicates that packets that are routed to the ME due to this filter will be sent to the HOST as well.
L24IPV63	21	RW	0b	Low IPv6 address 3 (L24IPV63) When set indicates that packets that are routed to the ME due to this filter will be sent to the HOST as well.
FP4	22	RW	0b	Flex Port 4 (FP4) When set indicates that packets that are routed to the ME due to this filter will be sent to the HOST as well.
FP5	23	RW	0b	Flex Port 5 (FP5) When set indicates that packets that are routed to the ME due to this filter will be sent to the HOST as well.
ICMP_IPV4	24	RW	0b	ICMP_IPV4 When set indicates that packets that are routed to the ME due to this filter will be sent to the HOST as well.
IPV4	25	RW	0b	IPV4 When set indicates that packets that are routed to the ME due to this filter will be sent to the HOST as well.
FP6	26	RW	0b	Flex Port 6 (FP6) When set indicates that packets that are routed to the ME due to this filter will be sent to the HOST as well.
FP7	27	RW	0b	Flex Port 7 (FP7) When set indicates that packets that are routed to the ME due to this filter will be sent to the HOST as well.
FP8	28	RW	0b	Flex Port 8 (FP8) When set indicates that packets that are routed to the ME due to this filter will be sent to the HOST as well.
FP9	29	RW	0b	Flex Port 9 (FP9) When set indicates that packets that are routed to the ME due to this filter will be sent to the HOST as well.
FP10	30	RW	0b	Flex Port 10 (FP10) When set indicates that packets that are routed to the ME due to this filter will be sent to the HOST as well.
FP11	31	RW	0b	Flex Port 11 (FP11) When set indicates that packets that are routed to the ME due to this filter will be sent to the HOST as well.





### 9.5.9.2.57 Management 2 Host Control Register 2 – MANC2H2 PHY Address 01, Page 801, Registers 32-33

Field Name	Bit(s)	Type	Default	Description
TCPPORT0	0	RW	0b	When set indicates that packets that are routed to the ME due to this filter will be sent to the HOST as well.
TCPPORT1	1	RW	0b	When set indicates that packets that are routed to the ME due to this filter will be sent to the HOST as well.
TCPPORT2	2	RW	0b	When set indicates that packets that are routed to the ME due to this filter will be sent to the HOST as well.
TCPPORT3	3	RW	0b	When set indicates that packets that are routed to the ME due to this filter will be sent to the HOST as well.
TCPPORT4	4	RW	0b	When set indicates that packets that are routed to the ME due to this filter will be sent to the HOST as well.
TCPPORT5	5	RW	0b	When set indicates that packets that are routed to the ME due to this filter will be sent to the HOST as well.
TCPPORT6	6	RW	0b	When set indicates that packets that are routed to the ME due to this filter will be sent to the HOST as well.
TCPPORT7	7	RW	0b	When set indicates that packets that are routed to the ME due to this filter will be sent to the HOST as well.
TCPPORT8	8	RW	0b	When set indicates that packets that are routed to the ME due to this filter will be sent to the HOST as well.
TCPPORT9	9	RW	0b	When set indicates that packets that are routed to the ME due to this filter will be sent to the HOST as well.
TCPPORT10	10	RW	0b	When set indicates that packets that are routed to the ME due to this filter will be sent to the HOST as well.
Reserved	11	RO	0b	Reserved.
UDPPORT0	12	RW	0b	When set indicates that packets that are routed to the ME due to this filter will be sent to the HOST as well.
DHCPv6	13	RW	0b	When set indicates that packets that are routed to the ME due to this filter will be sent to the HOST as well.
EAPoUDP	14	RW	0b	When set indicates that packets that are routed to the ME due to this filter will be sent to the HOST as well.
DNS	15	RW	0b	When set indicates that packets that are routed to the ME due to this filter will be sent to the HOST as well.
UDPIPPORT0	16	RW	0b	When set indicates that packets that are routed to the ME due to this filter will be sent to the HOST as well.
Reserved	17	RO	0b	Reserved.
UDPIPPORT1	18	RW	0b	When set indicates that packets that are routed to the ME due to this filter will be sent to the HOST as well.



Field Name	Bit(s)	Type	Default	Description
Reserved	19	RO	0b	Reserved.
UDPIPPORT2	20	RW	0b	When set indicates that packets that are routed to the ME due to this filter will be sent to the HOST as well.
Reserved	21	RO	0b	Reserved.
UDPIPPORT3	22	RW	0b	When set indicates that packets that are routed to the ME due to this filter will be sent to the HOST as well.
Reserved	23	RO	0b	Reserved.
MRFUTPF	24	RW	0b	When set indicates that packets that are routed to the ME due to this filter will be sent to the HOST as well.
Host MTA	25	RW	0b	When set indicates that packets that are routed to the ME due to this filter will be sent to the HOST as well.
ICMPv6	26	RW	0b	When set indicates that packets that are routed to the ME due to this filter will be sent to the HOST as well.
Reserved	27	RO	0b	Reserved.
ETHERTYPE0	28	RW	0b	When set indicates that packets that are routed to the ME due to this filter will be sent to the HOST as well.
ETHERTYPE1	29	RW	0b	When set indicates that packets that are routed to the ME due to this filter will be sent to the HOST as well.
ETHERTYPE2	30	RW	0b	When set indicates that packets that are routed to the ME due to this filter will be sent to the HOST as well.
Reserved	31	RO	0b	Reserved.

### 9.5.9.2.58 IPv4 ME Binding Control – IPV4MBC PHY Address 01, Page 801, Registers 40-41

Field Name	Bit(s)	Type	Default	Description
EN_IPTCPORT0	0	RW	0b	Enable IP filter for TCPPORT0 (EN_IPTCPORT0) When set, only packets that match the ME IPv4 filter may pass TCPPORT0 filtering.
EN_IPTCPORT1	1	RW	0b	Enable IP filter for TCPPORT1 (EN_IPTCPORT1) When set, only packets that match the ME IPv4 filter may pass TCPPORT1 filtering.
EN_IPTCPORT2	2	RW	0b	Enable IP filter for TCPPORT2 (EN_IPTCPORT2) When set, only packets that match the ME IPv4 filter may pass TCPPORT2 filtering.
EN_IPTCPORT3	3	RW	0b	Enable IP filter for TCPPORT3 (EN_IPTCPORT3) When set, only packets that match the ME IPv4 filter may pass TCPPORT3 filtering.



Field Name	Bit(s)	Type	Default	Description
EN_IPTCPPORT4	4	RW	0b	Enable IP filter for TCPPORT4 (EN_IPTCPPORT4) When set, only packets that match the ME IPv4 filter may pass TCPPORT4 filtering.
EN_IPTCPPORT5	5	RW	0b	Enable IP filter for TCPPORT5 (EN_IPTCPPORT5) When set, only packets that match the ME IPv4 filter may pass TCPPORT5 filtering.
EN_IPTCPPORT6	6	RW	0b	Enable IP filter for TCPPORT6 (EN_IPTCPPORT6) When set, only packets that match the ME IPv4 filter may pass TCPPORT6 filtering.
EN_IPTCPPORT7	7	RW	0b	Enable IP filter for TCPPORT7 (EN_IPTCPPORT7) When set, only packets that match the ME IPv4 filter may pass TCPPORT7 filtering.
EN_IPTCPPORT8	8	RW	0b	Enable IP filter for TCPPORT8 (EN_IPTCPPORT8) When set, only packets that match the ME IPv4 filter may pass TCPPORT8 filtering.
EN_IPTCPPORT9	9	RW	0b	Enable IP filter for TCPPORT9 (EN_IPTCPPORT9) When set, only packets that match the ME IPv4 filter may pass TCPPORT9 filtering.
EN_IPTCPPORT10	10	RW	0b	Enable IP filter for TCPPORT10 (EN_IPTCPPORT10) When set, only packets that match the ME IPv4 filter may pass TCPPORT10 filtering.
Reserved	11	RO	0b	Reserved
EN_IPUDPPORT0	12	RW	0b	Enable IP filter for UDPPORT0 (EN_IPUDPPORT0) When set, only packets that match the ME IPv4 filter may pass UDPPORT0 filtering.
Reserved	13	RO	0b	Reserved
EN_IPEAPoUDP	14	RW	0b	Enable IP filter for EAPoUDP (EN_IPEAPoUDP) When set, only packets that match the ME IPv4 filter may pass EAPoUDP filtering.
EN_IPDNS	15	RW	0b	Enable IP filter for DNS (EN_IPDNS) When set, only packets that match the ME IPv4 filter may pass DNS filtering.
EN_IPFLEX0	16	RW	0b	Enable IP filter for Flex port 0 (EN_IPFLEX0) When set, only packets that match the ME IPv4 filter may pass flex port 0 filtering.
EN_IPFLEX1	17	RW	0b	Enable IP filter for Flex port 1 (EN_IPFLEX1) When set, only packets that match the ME IPv4 filter may pass flex port 1 filtering.
EN_IPFLEX2	18	RW	0b	Enable IP filter for Flex port 2 (EN_IPFLEX2) When set, only packets that match the ME IPv4 filter may pass flex port 2 filtering.



Field Name	Bit(s)	Type	Default	Description
EN_IPFLEX3	19	RW	0b	Enable IP filter for Flex port 3 (EN_IPFLEX3) When set, only packets that match the ME IPv4 filter may pass flex port 3 filtering.
EN_IPFLEX4	20	RW	0b	Enable IP filter for Flex port 4 (EN_IPFLEX4) When set, only packets that match the ME IPv4 filter may pass flex port 4 filtering.
EN_IPFLEX5	21	RW	0b	Enable IP filter for Flex port 5 (EN_IPFLEX5) When set, only packets that match the ME IPv4 filter may pass flex port 5 filtering.
EN_IPFLEX6	22	RW	0b	Enable IP filter for Flex port 6 (EN_IPFLEX6) When set, only packets that match the ME IPv4 filter may pass flex port 6 filtering.
EN_IPFLEX7	23	RW	0b	Enable IP filter for Flex port 7 (EN_IPFLEX7) When set, only packets that match the ME IPv4 filter may pass flex port 7 filtering.
EN_IPFLEX8	24	RW	0b	Enable IP filter for Flex port 8 (EN_IPFLEX8) When set, only packets that match the ME IPv4 filter may pass flex port 8 filtering.
EN_IPFLEX9	25	RW	0b	Enable IP filter for Flex port 9 (EN_IPFLEX9) When set, only packets that match the ME IPv4 filter may pass flex port 9 filtering.
EN_IPFLEX10	26	RW	0b	Enable IP filter for Flex port 10 (EN_IPFLEX10) When set, only packets that match the ME IPv4 filter may pass flex port 10 filtering.
EN_IPFLEX11	27	RW	0b	Enable IP filter for Flex port 11 (EN_IPFLEX11) When set, only packets that match the ME IPv4 filter may pass flex port 11 filtering.
EN_IPMRFUTPF	28	RW	0b	Enable IP filter for MRFUTPF (EN_IPMRFUTPF) When set, only packets that match the ME IPv4 filter may pass MRFUTPF range port filtering.
EN_IPICMPv4	29	RW	0b	Enable IP filter for ICMPv4 (EN_IPICMPv4) When set, only packets that match the ME IPv4 filter may pass ICMPv4 filtering.
EN_IPARP	30	RW	0b	Enable IP filter for ARP (EN_IPARP) When set, only packets that match the ME IPv4 filter may pass ARP request filtering.
EN_IPRMCP	31	RW	0b	Enable IP filter for RMCP (EN_IPRMCP) When set, only packets that match the ME IPv4 filter may pass RMCP filtering.



### 9.5.9.2.59 IPv4 Host Binding Control – IPV4HBC PHY Address 01, Page 801, Registers 42-43

Field Name	Bit(s)	Type	Default	Description
EN_IPTCPPORT0	0	RW	0b	Enable IP filter for TCPPORT0 (EN_IPTCPPORT0) When set, only packets that match the Host IPv4 filters may pass TCPPORT0 filtering.
EN_IPTCPPORT1	1	RW	0b	Enable IP filter for TCPPORT1 (EN_IPTCPPORT1) When set, only packets that match the Host IPv4 filters may pass TCPPORT1 filtering.
EN_IPTCPPORT2	2	RW	0b	Enable IP filter for TCPPORT2 (EN_IPTCPPORT2) When set, only packets that match the Host IPv4 filters may pass TCPPORT2 filtering.
EN_IPTCPPORT3	3	RW	0b	Enable IP filter for TCPPORT3 (EN_IPTCPPORT3) When set, only packets that match the Host IPv4 filters may pass TCPPORT3 filtering.
EN_IPTCPPORT4	4	RW	0b	Enable IP filter for TCPPORT4 (EN_IPTCPPORT4) When set, only packets that match the Host IPv4 filters may pass TCPPORT4 filtering.
EN_IPTCPPORT5	5	RW	0b	Enable IP filter for TCPPORT5 (EN_IPTCPPORT5) When set, only packets that match the Host IPv4 filters may pass TCPPORT5 filtering.
EN_IPTCPPORT6	6	RW	0b	Enable IP filter for TCPPORT6 (EN_IPTCPPORT6) When set, only packets that match the Host IPv4 filters may pass TCPPORT6 filtering.
EN_IPTCPPORT7	7	RW	0b	Enable IP filter for TCPPORT7 (EN_IPTCPPORT7) When set, only packets that match the Host IPv4 filters may pass TCPPORT7 filtering.
EN_IPTCPPORT8	8	RW	0b	Enable IP filter for TCPPORT8 (EN_IPTCPPORT8) When set, only packets that match the Host IPv4 filters may pass TCPPORT8 filtering.
EN_IPTCPPORT9	9	RW	0b	Enable IP filter for TCPPORT9 (EN_IPTCPPORT9) When set, only packets that match the Host IPv4 filters may pass TCPPORT9 filtering.
EN_IPTCPPORT10	10	RW	0b	Enable IP filter for TCPPORT10 (EN_IPTCPPORT10) When set, only packets that match the Host IPv4 filters may pass TCPPORT10 filtering.
Reserved	11	RO	0b	Reserved
EN_IPUDPPORT0	12	RW	0b	Enable IP filter for UDPPORT0 (EN_IPUDPPORT0) When set, only packets that match the Host IPv4 filters may pass UDPPORT0 filtering.
Reserved	13	RO	0b	Reserved



Field Name	Bit(s)	Type	Default	Description
EN_IPEAPoUDP	14	RW	0b	Enable IP filter for EAPoUDP (EN_IPEAPoUDP) When set, only packets that match the Host IPv4 filters may pass EAPoUDP filtering.
EN_IPDNS	15	RW	0b	Enable IP filter for DNS (EN_IPDNS) When set, only packets that match the Host IPv4 filters may pass DNS filtering.
EN_IPFLEX0	16	RW	0b	Enable IP filter for Flex port 0 (EN_IPFLEX0) When set, only packets that match the Host IPv4 filters may pass flex port 0 filtering.
EN_IPFLEX1	17	RW	0b	Enable IP filter for Flex port 1 (EN_IPFLEX1) When set, only packets that match the Host IPv4 filters may pass flex port 1 filtering.
EN_IPFLEX2	18	RW	0b	Enable IP filter for Flex port 2 (EN_IPFLEX2) When set, only packets that match the Host IPv4 filters may pass flex port 2 filtering.
EN_IPFLEX3	19	RW	0b	Enable IP filter for Flex port 3 (EN_IPFLEX3) When set, only packets that match the Host IPv4 filters may pass flex port 3 filtering.
EN_IPFLEX4	20	RW	0b	Enable IP filter for Flex port 4 (EN_IPFLEX4) When set, only packets that match the Host IPv4 filters may pass flex port 4 filtering.
EN_IPFLEX5	21	RW	0b	Enable IP filter for Flex port 5 (EN_IPFLEX5) When set, only packets that match the Host IPv4 filters may pass flex port 5 filtering.
EN_IPFLEX6	22	RW	0b	Enable IP filter for Flex port 6 (EN_IPFLEX6) When set, only packets that match the Host IPv4 filter may pass flex port 6 filtering.
EN_IPFLEX7	23	RW	0b	Enable IP filter for Flex port 7 (EN_IPFLEX7) When set, only packets that match the Host IPv4 filters may pass flex port 7 filtering.
EN_IPFLEX8	24	RW	0b	Enable IP filter for Flex port 8 (EN_IPFLEX8) When set, only packets that match the Host IPv4 filters may pass flex port 8 filtering.
EN_IPFLEX9	25	RW	0b	Enable IP filter for Flex port 9 (EN_IPFLEX9) When set, only packets that match the Host IPv4 filters may pass flex port 9 filtering.
EN_IPFLEX10	26	RW	0b	Enable IP filter for Flex port 10 (EN_IPFLEX10) When set, only packets that match the Host IPv4 filters may pass flex port 10 filtering.
EN_IPFLEX11	27	RW	0b	Enable IP filter for Flex port 11 (EN_IPFLEX11) When set, only packets that match the Host IPv4 filters may pass flex port 11 filtering.



Field Name	Bit(s)	Type	Default	Description
EN_IPMRFUTPF	28	RW	0b	Enable IP filter for MRFUTPF (EN_IPMRFUTPF) When set, only packets that match the Host IPv4 filters may pass MRFUTPF range port filtering.
EN_IPICMPv4	29	RW	0b	Enable IP filter for ICMPv4 (EN_IPICMPv4) When set, only packets that match the Host IPv4 filters may pass ICMPv4 filtering.
EN_IPARP	30	RW	0b	Enable IP filter for ARP (EN_IPARP) When set, only packets that match the Host IPv4 filters may pass ARP request filtering.
EN_IPRMCP	31	RW	0b	Enable IP filter for RMCP (EN_IPRMCP) When set, only packets that match the Host IPv4 filters may pass RMCP filtering.

### 9.5.9.2.60 IPv6 Binding Control – IPV6BC PHY Address 01, Page 801, Registers 50-51

Field Name	Bit(s)	Type	Default	Description
EN_IPTCPORT0	0	RW	0b	Enable IP filter for TCPPORT0 (EN_IPTCPORT0) When set, only packets that match the L24IPV6 filters may pass TCPPORT0 filtering.
EN_IPTCPORT1	1	RW	0b	Enable IP filter for TCPPORT1 (EN_IPTCPORT1) When set, only packets that match the L24IPV6 filters may pass TCPPORT1 filtering.
EN_IPTCPORT2	2	RW	0b	Enable IP filter for TCPPORT2 (EN_IPTCPORT2) When set, only packets that match the L24IPV6 filters may pass TCPPORT2 filtering.
EN_IPTCPORT3	3	RW	0b	Enable IP filter for TCPPORT3 (EN_IPTCPORT3) When set, only packets that match the L24IPV6 filters may pass TCPPORT3 filtering.
EN_IPTCPORT4	4	RW	0b	Enable IP filter for TCPPORT4 (EN_IPTCPORT4) When set, only packets that match the L24IPV6 filters may pass TCPPORT4 filtering.
EN_IPTCPORT5	5	RW	0b	Enable IP filter for TCPPORT5 (EN_IPTCPORT5) When set, only packets that match the L24IPV6 filters may pass TCPPORT5 filtering.
EN_IPTCPORT6	6	RW	0b	Enable IP filter for TCPPORT6 (EN_IPTCPORT6) When set, only packets that match the L24IPV6 filters may pass TCPPORT6 filtering.
EN_IPTCPORT7	7	RW	0b	Enable IP filter for TCPPORT7 (EN_IPTCPORT7) When set, only packets that match the L24IPV6 filters may pass TCPPORT7 filtering.



Field Name	Bit(s)	Type	Default	Description
EN_IPTCPPT8	8	RW	0b	Enable IP filter for TCPPT8 (EN_IPTCPPT8) When set, only packets that match the L24IPV6 filters may pass TCPPT8 filtering.
EN_IPTCPPT9	9	RW	0b	Enable IP filter for TCPPT9 (EN_IPTCPPT9) When set, only packets that match the L24IPV6 filters may pass TCPPT9 filtering.
EN_IPTCPPT10	10	RW	0b	Enable IP filter for TCPPT10 (EN_IPTCPPT10) When set, only packets that match the L24IPV6 filters may pass TCPPT10 filtering.
Reserved	11	RO	0b	Reserved
EN_IPUDPT0	12	RW	0b	Enable IP filter for UDPT0 (EN_IPUDPT0) When set, only packets that match the L24IPV6 filters may pass UDPT0 filtering.
EN_IPDHCPv6	13	RW	0b	Enable IP filter for DHCPv6 (EN_IPDHCPv6) When set, only packets that match the L24IPV6 filters may pass DHCPv6 filtering.
EN_IPEAPoUDP	14	RW	0b	Enable IP filter for EAPoUDP (EN_IPEAPoUDP) When set, only packets that match the L24IPV6 filters may pass EAPoUDP filtering.
EN_IPDNS	15	RW	0b	Enable IP filter for DNS (EN_IPDNS) When set, only packets that match the L24IPV6 filters may pass DNS filtering.
EN_IPFLEX0	16	RW	0b	Enable IP filter for Flex port 0 (EN_IPFLEX0) When set, only packets that match the L24IPV6 filters may pass flex port 0 filtering.
EN_IPFLEX1	17	RW	0b	Enable IP filter for Flex port 1 (EN_IPFLEX1) When set, only packets that match the L24IPV6 filters may pass flex port 1 filtering.
EN_IPFLEX2	18	RW	0b	Enable IP filter for Flex port 2 (EN_IPFLEX2) When set, only packets that match the L24IPV6 filters may pass flex port 2 filtering.
EN_IPFLEX3	19	RW	0b	Enable IP filter for Flex port 3 (EN_IPFLEX3) When set, only packets that match the L24IPV6 filters may pass flex port 3 filtering.
EN_IPFLEX4	20	RW	0b	Enable IP filter for Flex port 4 (EN_IPFLEX4) When set, only packets that match the L24IPV6 filters may pass flex port 4 filtering.
EN_IPFLEX5	21	RW	0b	Enable IP filter for Flex port 5 (EN_IPFLEX5) When set, only packets that match the L24IPV6 filters may pass flex port 5 filtering.
EN_IPFLEX6	22	RW	0b	Enable IP filter for Flex port 6 (EN_IPFLEX6) When set, only packets that match the L24IPV6 filter may pass flex port 6 filtering.





Field Name	Bit(s)	Type	Default	Description
EN_IPFLEX7	23	RW	0b	Enable IP filter for Flex port 7 (EN_IPFLEX7) When set, only packets that match the L24IPV6 filters may pass flex port 7 filtering.
EN_IPFLEX8	24	RW	0b	Enable IP filter for Flex port 8 (EN_IPFLEX8) When set, only packets that match the L24IPV6 filters may pass flex port 8 filtering.
EN_IPFLEX9	25	RW	0b	Enable IP filter for Flex port 9 (EN_IPFLEX9) When set, only packets that match the L24IPV6 filters may pass flex port 9 filtering.
EN_IPFLEX10	26	RW	0b	Enable IP filter for Flex port 10 (EN_IPFLEX10) When set, only packets that match the L24IPV6 filters may pass flex port 10 filtering.
EN_IPFLEX11	27	RW	0b	Enable IP filter for Flex port 11 (EN_IPFLEX11) When set, only packets that match the L24IPV6 filters may pass flex port 11 filtering.
EN_IPMRFUTPF	28	RW	0b	Enable IP filter for MRFUTPF (EN_IPMRFUTPF) When set, only packets that match the L24IPV6 filters may pass MRFUTPF range port filtering.
EN_IPICMPv4	29	RW	0b	Enable IP filter for ICMPv4 (EN_IPICMPv4) When set, only packets that match the L24IPV6 filters may pass ICMPv4 filtering.
Reserved	30	RO	0b	Reserved.
EN_IPRMCP	31	RW	0b	Enable IP filter for RMCP (EN_IPRMCP) When set, only packets that match the L24IPV6 filters may pass RMCP filtering.

#### 9.5.9.2.61 SHRA Filter Enable Register – SHRAFER PHY Address 01, Page 801, Register 52

Field Name	Bit(s)	Type	Default	Description
EN_SHRA0_FILTER	0	RW	0b	Enables Shared MAC address filtering. When this bit set and the AV bit is set in the SHRAH[0] register and the Rx packet matches SHRA[0] the packet will be routed to the ME.
EN_SHRA1_FILTER	1	RW	0b	Enables Shared MAC address filtering. When this bit set and the AV bit is set in the SHRAH[1] register and the Rx packet matches SHRA[1] the packet will be routed to the ME.
EN_SHRA2_FILTER	2	RW	0b	Enables Shared MAC address filtering. When this bit set and the AV bit is set in the SHRAH[2] register and the Rx packet matches SHRA[2] the packet will be routed to the ME.
EN_SHRA3_FILTER	3	RW	0b	Enables Shared MAC address filtering. When this bit set and the AV bit is set in the SHRAH[3] register and the Rx packet matches SHRA[3] the packet will be routed to the ME.



Field Name	Bit(s)	Type	Default	Description
EN_SHRA4_FILTER	4	RW	0b	Enables Shared MAC address filtering. When this bit set and the AV bit is set in the SHRAH[4] register and the Rx packet matches SHRA[4] the packet will be routed to the ME.
EN_SHRA5_FILTER	5	RW	0b	Enables Shared MAC address filtering. When this bit set and the AV bit is set in the SHRAH[5] register and the Rx packet matches SHRA[5] the packet will be routed to the ME.
EN_SHRA6_FILTER	6	RW	0b	Enables Shared MAC address filtering. When this bit set and the AV bit is set in the SHRAH[6] register and the Rx packet matches SHRA[6] the packet will be routed to the ME.
EN_SHRA7_FILTER	7	RW	0b	Enables Shared MAC address filtering. When this bit set and the AV bit is set in the SHRAH[7] register and the Rx packet matches SHRA[7] the packet will be routed to the ME.
EN_SHRA8_FILTER	8	RW	0b	Enables Shared MAC address filtering. When this bit set and the AV bit is set in the SHRAH[8] register and the Rx packet matches SHRA[8] the packet will be routed to the ME.
EN_SHRA9_FILTER	9	RW	0b	Enables Shared MAC address filtering. When this bit set and the AV bit is set in the SHRAH[9] register and the Rx packet matches SHRA[9] the packet will be routed to the ME.
EN_SHRA10_FILTER	10	RW	0b	Enables Shared MAC address filtering. When this bit set and the AV bit is set in the SHRAH[10] register and the Rx packet matches SHRA[10] the packet will be routed to the ME.
Reserved	15:11	RO	0x0	Reserved.

## 9.5.10 Proxy Controller uCode

### 9.5.10.1 Proxy Micro Code – PMC PHY Address 01, Page 802, Register 0-1536

Field Name	Bit(s)	Type	Default	Description
Micro Code	15:0	RW	0x00	Micro code.



## 9.5.11 Host WoL Packet

### 9.5.11.1 Host WoL Packet Data – HWPDPH Address 01, Page 803, Register 0-63

Field Name	Bit(s)	Type	Default	Description
	15:0	RO	0x00	Host WoL captured packet data.

### 9.5.11.2 Host WoL Packet Length – HWPLPH Address 01, Page 803, Register 64

Field Name	Bit(s)	Type	Default	Description
	15:0	RO	0x00	Host WoL captured packet Length. A value of 0x00 means no packet was captured.

### 9.5.11.3 Host WoL Packet Clear – HWPCPH Address 01, Page 803, Register 66

Field Name	Bit(s)	Type	Default	Description
	15:0	RO	0x00	Host WoL packet Indication clear. Register accessed by read/write to clear the WoL packet indication. Reads always return 0x0000.



## 9.5.12 LPI MMD PHY Registers

LPI MMD PHY registers are part of the I219's EMI registers. These registers are accessed via MDIO by programming the EMI address to register MI16 and reading/writing the data from/to register MI17.

### 9.5.12.1 I219 EMI Registers PHY Address 02, Page 0, Registers 16-17

IEEE MMD	MMD Bits	EMI Address	EMI Bits	Type	Description
3.0	10	9400	10		Clock stoppable.
3.1	11	9401	11		Tx LP idle received.
3.1	10	9401	10		Rx LP idle received
3.1	9	9401	9		Tx LP idle indication
3.1	8	9401	8		RX LP idle indication
3.20	15:0	8000	15:0		EEE capability register
3.22	15:0	A000	15:0		EEE wake error counter in 100BASE-TX mode
3.22	15:0	A000	15:0		EEE wake error counter in 1000BASE-T mode
7.60	15:0	8001	15:0		EEE advertisement
7.61	15:0	8002	15:0		EEE LP advertisement



## 10.0 Non-Volatile Memory (NVM)

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### 10.1 Introduction

This section is intended for designs using a 10/100/1000 Mb/s Intel® C220 Series Chipset integrated LAN controller in conjunction with the Intel® Ethernet Connection I219.

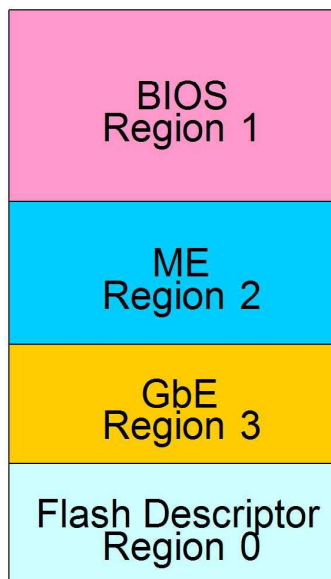
There are several LAN clients that might access the NVM such as hardware, LAN driver, and BIOS. Refer to the *Intel® C220 Series Chipset External Design Specification (Intel® C220 Series Chipset EDS)* and the *Intel® C220 Series Chipset SPI Programming Guide* for more details.

Unless otherwise specified, all numbers in this section use the following numbering convention:

- Numbers that do not have a suffix are decimal (base 10).
- Numbers with a prefix of "0x" are hexadecimal (base 16).
- Numbers with a suffix of "b" are binary (base 2).

### 10.2 NVM Programming Procedure Overview

The LAN NVM shares space on an SPI Flash device (or devices) along with the BIOS, Manageability Firmware, and a Flash Descriptor Region. It is programmed through the Intel® C220 Series Chipset. This combined image is shown in [Figure 10-1](#). The Flash Descriptor Region is used to define vendor specific information and the location, allocated space, and read and write permissions for each region. The Manageability (ME) Region contains the code and configuration data for ME functions such as Intel® Active Management Technology. The system BIOS is contained in the BIOS Region. The ME Region and BIOS Region are beyond the scope of this document and a more detailed explanation of these areas can be found in the *Intel® C220 Series Chipset Family External Design Specification (Intel® C220 Series Chipset EDS)*. This document describes the LAN image contained in the Gigabit Ethernet (GbE) region.



**Figure 10-1. LAN NVM Regions**

To access the NVM, it is essential to correctly setup the following:

1. A valid Flash Descriptor Region must be present. Details for the Flash Descriptor Region are contained in the *Intel® C220 Series Chipset EDS*. This process is described in detail in the *Intel® Active Management Technology OEM Bring-Up Guide*.

The *Intel® Active Management Technology OEM Bring-Up Guide* can be obtained by contacting your local Intel Field Service Representative.

2. The GbE region must be part of the original image flashed onto the part.
3. For Intel LAN tools and drivers to work correctly, the BIOS must set the VSCC register(s) correctly. There are two sets of VSCC registers, the upper (UVSCC) and lower (LVSCC). Note that the LVSCC register is only used if the NVM attributes change. For example, the use of a second flash component, a change in erase size between segments, etc. Due to the architecture of the Intel® C220 Series Chipset, if these registers are not set correctly, the LAN tools might not report an error message even though the NVM contents remain unchanged. Refer to the *Intel® C220 Series Chipset EDS* for more information



4. The GbE region of the NVM must be accessible. To keep this region accessible, the Protected Range register of the GbE LAN Memory Mapped Configuration registers must be set to their default value of 0x0000 0000. (The GbE Protected Range registers are described in the Intel® C220 Series Chipset EDS).
5. The sector size of the NVM must equal 256 bytes, 4 KB, or 64 KB. When a Flash device that uses a 64 KB sector erase is used, the GbE region size must equal 128 KB. If the Flash part uses a 4 KB or 256-byte sector erase, then the GbE region size must be set to 8 KB.

The NVM image contains both static and dynamic data. The static data is the basic platform configuration, and includes OEM specific configuration bits as well as the unique Printed Circuit Board Assembly (PBA). The dynamic data holds the product's Ethernet Individual Address (IA) and Checksum. This file can be created using a text editor.

## 10.3 LAN NVM Format and Contents

Table 10-1 lists the NVM maps for the LAN region. Each word listed is described in detail in the following sections.

**Table 10-1 LAN NVM Address Map**

LAN Word Offset	NVM Byte Offset	Used By	15 0	Image Value
0x00	0x00	HW-Shared	Ethernet Address Byte 2, 1	IA (2, 1) 0x8888
0x01	0x02	HW-Shared	Ethernet Address Byte 4, 3	IA (4, 3) 0x8888
0x02	0x04	HW-Shared	Ethernet Address Byte 6, 5	IA (6, 5) 0x8887
0x03	0x06	SW	Reserved	0x0800
0x04	0x08	SW	Reserved	0xFFFF
0x05	0x0A	SW	Image Version Information 1	Example: 0x0083 = minor revision 0x08 and image ID 0x3
0x06	0x0C	SW	EEPROM Track ID (Low)	0xFFFF: Example: 0x0048 in Intel -LP PCH NVM Rev 0.8
0x07	0x0E	SW	EEPROM Track ID (High)	0xFFFF: Example: 0x8000 in Intel -LP PCH NVM Rev 0.8
0x08	0x10	SW	PBA Low	0xFFFF
0x09	0x12	SW	PBA High	0xFFFF
0x0A	0x14	HW-PCI	PCI Init Control Word	0x10C3



LAN Word Offset	NVM Byte Offset	Used By	150	Image Value
0x0B	0x16	HW-PCI	Subsystem ID	0x0000
0x0C	0x18	HW-PCI	Subsystem Vendor ID	0x8086
0x0D	0x1A	HW-PCI	Device ID	0x156F for LM SKU (-LP PCH) or 0x15B7 for LM SKU (-H PCH)
0x0E	0x1C	HW-PCI	Reserved	0x0000
0x0F	0x1E	HW-PCI	Reserved	0x0000
0x10	0x20	HW-PCI	LAN Power Consumption	0x0000
0x11	0x22	HW	Reserved	0x0000
0x12	0x24		Reserved	0x8000
0x13	0x26	HW-Shared	Shared Init Control Word	0xA705
0x14	0x28	HW-Shared	Extended Configuration Word 1	0x302C
0x15	0x2A	HW-Shared	Extended Configuration Word 2	0x1000 (LAN Switch) 0x1600 (No-LAN Switch)
0x16	0x2C	HW-Shared	Extended Configuration Word 3	0x0000
0x17	0x2E	HW-Shared	LEDCTL 10EM Configuration Default	0x0000
0x18	0x30 (See note below.)	HW-Shared	LEDCTL 0 2 0 - 2	0x18F4 (Intel) or custom OEM setting
0x19:0x2F	0x32:0x5E	HW-Shared	Reserved	0xA000
0x30:0x3E	0x60:0x7C	PXE	PXE Software Region	0x0100
0x3F	0x7E	SW	Software Checksum (Bytes 0x00 through 0x7D)	0xFFFF
0x40:0x4A	0x80:0x94	HW	G3 -> S5 PHY Configuration	0x0000

Table notes:

- SW = Software: This is access from the network configuration tools and drivers.
- PXE = PXE Boot Agent: This is access from the PXE option ROM code in BIOS.
- HW-Shared = Hardware-Shared: This is read when the shared configuration is reset.
- HW-PCI = Hardware-PCI: This is read when the PCI Configuration is reset.





- Word 0x30: For more information, see *Intel® iSCSI Remote Boot Application Notes for BIOS Engineers*, Reference Number 322328.

## 10.3.1 Hardware Accessed Words

This section describes the NVM words that are loaded by the integrated LAN controller hardware.

### 10.3.1.1 Ethernet Address (Words 0x00-0x02)

The Ethernet Individual Address (IA) is a 6-byte field that must be unique for each Network Interface Card (NIC) or LAN on Motherboard (LOM), and thus unique for each copy of the NVM image. The first three bytes are vendor specific—for example, the IA is equal to [00 AA 00] or [00 A0 C9] for Intel products. The value from this field is loaded into the Receive Address Register 0 (RAL0/RAH0).

For the purpose of this section, the IA byte numbering convention is indicated as follows; byte 1, bit 0 is first on the wire and byte 6, bit 7 is last. Note that byte 1, bit 0 is the unicast/multicast address indication while zero means unicast address. Byte 1, bit 1 identifies the global/local indication while zero means a global address.

	IA Byte/Value					
Vendor	1	2	3	4	5	6
Intel Original	00	AA	00	variable	variable	variable
Intel New	00	A0	C9	variable	variable	variable

### 10.3.1.2 PCI Init Control Word (Word 0x0A)

This word contains initialization values that:

- Set defaults for some internal registers
- Enable/disable specific features
- Determines which PCI configuration space values are loaded from the NVM

Bit	Name	Default	Description
15:14	Reserved	00b	Reserved
13:12	Reserved	01b	Reserved
11:8	Reserved	0x0	Reserved



Bit	Name	Default	Description
7	AUX PWR	1b	Auxiliary Power Indication If set and if PM Ena is set, D3cold wake-up is advertised in the PCH register of the PCI function. 0b = No AUX power. 1b = AUX power.
6	PM Enable	1b	Power Management Enable (PME-WoL) Enables asserting PME in the PCI function at any power state. This bit affects the advertised PME_Support indication in the PCH register of the PCI function. 0b = Disable. 1b = Enable.
5:4	Reserved	0x0	These bits are reserved and must be set to 0x0.
3	ENABLE_SSID_UP	0b	Enable SSID write once by the host
2		0b	Reserved
1	Load Subsystem IDs	1b	Load Subsystem IDs from NVM When set to 1b, indicates that the device is to load its PCI Subsystem ID and Subsystem Vendor ID from the NVM (words 0x0B and 0x0C).
0	Load Device IDs	1b	Load Device ID from NVM When set to 1b, indicates that the device is to load its PCI Device ID from the NVM (word 0x0D).

### 10.3.1.3 Subsystem ID (Word 0x0B)

If the Load Subsystem ID in word 0x0A is set, this word is read-in to initialize the Subsystem ID. Default value is 0x0000.

### 10.3.1.4 Subsystem Vendor ID (Word 0x0C)

If the Load Subsystem ID in word 0x0A is set, this word is read-in to initialize the Subsystem Vendor ID. Default value is 0x8086.

### 10.3.1.5 Device ID (Word 0x0D)

If the Load Device ID in word 0x0A is set, this word is read-in to initialize the Device ID of the I219LM PHY. Default value is 0x156F.

**Note:** When the I219V SKU is used in combination with certain chipset SKUs, the default value for this word is 0x15B7.



### 10.3.1.6 Words 0x0E and 0x0F Are Reserved

Default value is 0x0.

**Note:** In some OEM custom images these words are used for adding the track ID.

Bits	Name	Default	Description
15:8	Reserved	0x00	Reserved, must be set to 0x00.
7:0	DEVREVID	0x00	Device Rev ID. The actual device revision ID is the NVM value XORed with the default value of I219.

### 10.3.1.7 LAN Power Consumption (Word 0x10)

This word is meaningful only if the power management is enabled. The default value is 0x0702.

Bits	Name	Default	Description
15:8	LAN D0 Power	0x7	The value in this field is reflected in the PCI Power Management Data register for D0 power consumption and dissipation ( <i>Data_Select</i> = 0 or 4). Power is defined in 100 mW units. The power also includes the external logic required for the LAN function.
7:5	Reserved	000b	Reserved, set to 000b.
4:0	LAN D3 Power	0x1	The value in this field is reflected in the PCI Power Management Data register for D3 power consumption and dissipation ( <i>Data_Select</i> = 3 or 7). Power is defined in 100 mW units. The power also includes the external logic required for the LAN function. The most significant bits in the Data register that reflects the power values are padded with zeros.

### 10.3.1.8 Word 0x11 and Word 0x12 Are Reserved

Bits	Name	Default	Description
15:0	Reserved	0x0000	Reserved, set to 0x0000.



### 10.3.1.9 Shared Init Control Word (Word 0x13)

This word controls general initialization values.

Bits	Name	Default	Description
15:14	Sign	10b	<b>Valid Indication</b> A 2-bit valid indication field indicates to the device that there is a valid NVM present. If the valid field does not equal 10b the integrated LAN controller does not read the rest of the NVM data and default values are used for the device configuration.
13:11	Reserved	0x0	Reserved.
10	Reserved	1b	Reserved, set to 1b.
9	PHY PD Ena	01	<b>Enable PHY Power Down</b> When set, enables PHY power down at DMoff/D3 or Dr and no WoL. This bit is loaded to the <i>PHY Power Down Enable</i> bit in the Extended Device Control (CTRL_EXT) register. 1b = Enable PHY power down. 0b = PHY always powered up.
8	Reserved	1b	Reserved, should be set to 1b.
7:6	PHYT	00b	<b>PHY Device Type</b> Indicates that the PHY is connected to the integrated LAN controller and resulted mode of operation of the integrated LAN controller/PHY link buses. 00b = I219 01b = Reserved. 10b = Reserved. 11b = Reserved.
5	Reserved	0b	Reserved, should be set to 0b.
4	FRCSPD	0b	Default setting for the <i>Force Speed</i> bit in the Device Control register (CTRL[11]).
3	FD	0b	Default setting for the <i>Full Duplex</i> bit in the Device Control register (CTRL[0]). The hardware default value is 1b.
2	Reserved	1b	Reserved, set to 1b.
1	CLK_CNT_1_4	0b	When set, automatically reduces DMA frequency. Mapped to the Device Status register (STATUS[31]).
0	Dynamic Clock Gating	1b	When set, enables dynamic clock gating of the DMA and integrated LAN controller units. This bit is loaded to the <i>DynCK</i> bit in the CTRL_EXT register.



### 10.3.1.10 Extended Configuration Word 1 (Word 0x14)

Bits	Name	Default	Description
15:14	Reserved	00b	Reserved, set to 00b.
13	PHY Write Enable	1b	When set, enables loading of the extended PHY configuration area in the Lan Controller. When disabled, the extended PHY configuration area is ignored. Loaded to the EXTCNF_CTRL register.
12	OEM Write Enable	1b	When set, enables auto load of the OEM bits from the PHY_CTRL register to the PHY. Loaded to the Extended Configuration Control register (EXTCNF_CTRL[3]). 1b = OEM bits written to the Lan Controller 0b = No OEM bits configuration.
11:0	Extended Configuration Pointer	0x30	Defines the base address (in Dwords) of the Extended Configuration area in the NVM. The base address defines an offset value relative to the beginning of the LAN space in the NVM. A value of 0x00 is not supported when operating with the Lan Controller. Loaded to the Extended Configuration Control register (EXTCNF_CTRL[27:16]).

### 10.3.1.11 Extended Configuration Word 2 (Word 0x15)

Bits	Name	Default	Description
15:8	Extended PHY Length	0x0	Size (in Dwords) of the Extended PHY configuration area loaded to the Extended Configuration Size register (EXTCNF_SIZE[23:16]). If an extended configuration area is disabled by bit 13 in word 0x14, its length must be set to zero.
7:0	Reserved	0x0	Reserved, must be set to 0x00.

**Note:** This field is dependent upon the length of the extended configuration area. The default value above is for mobile images to be used on platforms with a LAN switch. Refer to the image relevant to the platform for the appropriate default value.

### 10.3.1.12 Extended Configuration Word 3 (Word 0x16)

Bits	Name	Default	Description
15:0	Reserved	0x00	Reserved, set to 0x00.



### 10.3.1.13 OEM Configuration Defaults (Word 0x17)

This word defines the OEM fields for the PHY power management parameters loaded to the PHY Control (PHY\_CTRL) register.

Bits	Name	Default	Description
15	B2B Enable	1b	Enable SPD in Back-to-Back Link setup
14	GbE Disable	0b	When set, GbE operation is disabled in all power states (including D0a).
13:12	Reserved	00b	Reserved, set to 00b.
11	GbE Disable in non-D0a	1b	Disables GbE operation in non-D0a states. This bit must be set if <i>GbE Disable</i> (bit 14) is set.
10	LPLU Enable in non-D0a	1b	Low Power Link Up Enables a reduction in link speed in non-D0a states when power policy and power management states are set to do so. This bit must be set if LPLU Enable in D0a bit is set.
9	LPLU Enable in D0a	0b	Low Power Link Up Enables a reduction in link speed in all power states.
8	SPD Enable	1	When set, enables PHY Smart Power Down mode.
7:0	Reserved	0x0	Reserved, set to 0x0.

### 10.3.1.14 LED 0—2 Configuration Defaults (Word 0x18)

This NVM word specifies the hardware defaults for the LED Control (LEDCTL) register fields controlling the LED1 (LINK\_1000), LED0 (LINK/ACTIVITY) and LED2 (LINK\_100) output behaviors. Refer to the *Intel® C220 Series Chipset Family PDG* and the *I219 Reference Schematics* for LED connection details. Mode encodings for LED outputs follow that.

**Note:** In all system states, the LEDs function as defined in Word 0x18 of the GbE region of the NVM after the software driver loads.

Bits	Name	Default	Description
15	Blink Rate	0b	<b>Blink Rate</b> 0b = Blink at 200 ms on and 200 ms off. 1b = Blink at 83 ms on and 83 ms off.
14	LED2 Blink	0b	<b>Initial Value of LED2_BLINK Field</b> 0b = Non-blinking. 1b = Blinking.
13	LED2 Invert	0b	<b>Initial Value of LED2_IVRT Field</b> 0b = Active-low output.



Bits	Name	Default	Description
12:10	LED2 Mode	110b	<b>LED2 Mode</b> Specifies what event/state/pattern is displayed on the LED2 output. 0110b = 100 Mb/s link_up.
9	LED1 Blink	0b	<b>Initial Value of LED1_BLINK Field</b> 0b = Non-blinking. 1b = Blinking.
8	LED1 Invert	0b	<b>Initial Value of LED1_IVRT Field</b> 0b = Active-low output.
7:5	LED1 Mode	111b	<b>LED1 Mode</b> Specifies what event/state/pattern is displayed on the LED1 output. 0111b = 1000 Mb/s link_up.
4	LED0 Blink	1b	<b>Initial Value of LED0_BLINK Field</b> 0b = Non-blinking. 1b = Blinking.
3	LED0 Invert	0b	<b>Initial Value of LED0_IVRT Field</b> 0b = Active-low output.
2:0	LED0 Mode	100b	<b>LED0 Mode</b> Specifies what event/state/pattern is displayed on the LED0 output. 100b = Filter activity on.



**Table 10-2 Mode Encodings for LED Outputs**

Mode	Mnemonic	State / Event Indicated
000b	LINK_10/1000	Asserted when either 10 or 1000 Mb/s link is established and maintained.
001b	LINK_100/1000	Asserted when either 100 or 1000 Mb/s link is established and maintained.
010b	LINK_UP	Asserted when any speed link is established and maintained.
011b	ACTIVITY	Asserted when link is established and packets are being transmitted or received.
100b	LINK/ACTIVITY	Asserted when link is established and when there is no transmit or receive activity.
101b	LINK_10	Asserted when a 10 Mb/s link is established and maintained.
110b	LINK_100	Asserted when a 100 Mb/s link is established and maintained.
111b	LINK_1000	Asserted when a 1000 Mb/s link is established and maintained.

### 10.3.1.15 Reserved (Word 0x19)

Bits	Name	Default	Description
15:0	Reserved	0x0A00	Reserved, set to 0x0A00.

### 10.3.1.16 Reserved (Word 0x1A)

Bits	Name	Default	Description
15:1	Reserved	0x0	Reserved, set to 0x0.
0	APM Enable	1b	APM Enable Initial value of Advanced Power Management Wake Up Enable in the Wake Up Control (WUC.APME) register. 1b = Advanced power management enabled. 0b = Advanced power management disabled.





### 10.3.1.17 Reserved (Word 0x1B)

Bits	Name	Default	Description
15:0	Reserved	0x0113	Reserved, set to 0x0113.

### 10.3.1.18 Reserved (Word 0x1C)

Bits	Name	Default	Description
15:0	Reserved	0x0	Reserved

### 10.3.1.19 Reserved (Word 0x1D)

Bits	Name	Default	Description
15:0	Reserved	0xBAAD	Reserved

### 10.3.1.20 Reserved (Word 0x1E)

Bits	Name	Default	Description
15:0	Reserved	0x0	Reserved

### 10.3.1.21 Reserved (Word 0x1F)

Bits	Name	Default	Description
15:0	Reserved	0x0	Reserved

### 10.3.1.22 Reserved (Word 0x20)

Bits	Name	Default	Description
15:0	Reserved	0xBAAD	Reserved



### 10.3.1.23 Reserved (Word 0x21)

Bits	Name	Default	Description
15:0	Reserved	0x0	Reserved

### 10.3.1.24 Reserved (Word 0x22)

Bits	Name	Default	Description
15:0	Reserved	0xBAAD	Reserved

### 10.3.1.25 Reserved (Word 0x23)

Bits	Name	Default	Description
15:0	Reserved	0x0	Reserved

### 10.3.1.26 Reserved (Word 0x24)

Bits	Name	Default	Description
15:0	Reserved	0x0	Reserved, set to 0x0.

### 10.3.1.27 Reserved (Word 0x25)

Bits	Name	Default	Description
15:0	Reserved	0x8080	Reserved, set to 0x8080

### 10.3.1.28 Reserved (Word 0x26)

Bits	Name	Default	Description
15:0	Reserved	0x4E00	Reserved, set to 0x4E00



### 10.3.1.29 Reserved (Word 0x27)

Bits	Name	Default	Description
15:0	Reserved	0x0886	Reserved

## 10.3.2 Software Accessed Words

### 10.3.2.1 PXE Words (Words 0x30 Through 0x3E)

Words 0x30 through 0x3E (bytes 0x60 through 0x7D) have been reserved for configuration and version values to be used by PXE code.

#### 10.3.2.1.1 Boot Agent Main Setup Options (Word 0x30)

The boot agent software configuration is controlled by the NVM with the main setup options stored in word 0x30. These options are those that can be changed by using the Control-S setup menu or by using the IBA Intel Boot Agent utility. Note that these settings only apply to Boot Agent software.



**Table 10-1 Boot Agent Main Setup Options**

Bit	Name	Default	Description
15:14	Reserved	00b	Reserved, set to 00b.
13	Reserved	0b	Reserved, must be set to 0b.
12	FDP	0b	Force Full Duplex. Set this bit to 0b for half duplex and 1b for full duplex. Note that this bit is a don't care unless bits 10 and 11 are set.
11:10	FSP	00b	Force Speed. These bits determine speed. 01b = 10 Mb/s. 10b = 100 Mb/s. 11b = Not allowed. All zeros indicate auto-negotiate (the current bit state). Note that bit 12 is a don't care unless these bits are set.
9	Reserved	0b	Reserved Set this bit to 0b.
8	DSM	1b	Display Setup Message. If this bit is set to 1b, the "Press Control-S" message appears after the title message. The default for this bit is 1b.
7:6	PT	00b	Prompt Time. These bits control how long the "Press Control-S" setup prompt message appears, if enabled by DIM. 00b = 2 seconds (default). 01b = 3 seconds. 10b = 5 seconds. 11b = 0 seconds. Note that the Ctrl-S message does not appear if 0 seconds prompt time is selected.
5	Reserved	0b	Reserved
4:3	DBS	00b	Default Boot Selection. These bits select which device is the default boot device. These bits are only used if the agent detects that the BIOS does not support boot order selection or if the MODE field of word 0x31 is set to MODE_LEGACY. 00b = Network boot, then local boot. 01b = Local boot, then network boot. 10b = Network boot only. 11b = Local boot only.



Bit	Name	Default	Description
2	Reserved	0b	Reserved
1:0	PS	00b	Protocol Select. These bits select the boot protocol. 00b = PXE (default value). 01b = Reserved. Other values are undefined.

### 10.3.2.1.2 Boot Agent Configuration Customization Options (Word 0x31)

Word 0x31 contains settings that can be programmed by an OEM or network administrator to customize the operation of the software. These settings cannot be changed from within the Control-S setup menu or the IBA Intel Boot Agent utility. The lower byte contains settings that would typically be configured by a network administrator using the Intel Boot Agent utility; these settings generally control which setup menu options are changeable. The upper byte are generally settings that would be used by an OEM to control the operation of the agent in a LOM environment, although there is nothing in the agent to prevent their use on a NIC implementation.



**Table 10-1 Boot Agent Configuration Customization Options (Word 0x31)**

Bit	Name	Default	Description
15:14	SIG	01b	Signature Set these bits to 11b to indicate valid data.
13:12	Reserved	00b	Reserved, must be set to 00b.
11		0b	Continuous Retry Disabled (0b default).
10:8	MODE	0x0	<p>Selects the agent's boot order setup mode. This field changes the agent's default behavior in order to make it compatible with systems that do not completely support the BBS and PnP Expansion ROM standards. Valid values and their meanings are:</p> <p>000b = Normal behavior. The agent attempts to detect BBS and PnP Expansion ROM support as it normally does.</p> <p>001b = Force Legacy mode. The agent does not attempt to detect BBS or PnP Expansion ROM supports in the BIOS and assumes the BIOS is not compliant. The BIOS boot order can be changed in the Setup Menu.</p> <p>010b = Force BBS mode. The agent assumes the BIOS is BBS-compliant, even though it might not be detected as such by the agent's detection code. The BIOS boot order CANNOT be changed in the Setup Menu.</p> <p>011b = Force PnP Int18 mode. The agent assumes the BIOS allows boot order setup for PnP Expansion ROMs and hooks interrupt 18h (to inform the BIOS that the agent is a bootable device) in addition to registering as a BBS IPL device. The BIOS boot order CANNOT be changed in the Setup Menu.</p> <p>100b = Force PnP Int19 mode. The agent assumes the BIOS allows boot order setup for PnP Expansion ROMs and hooks interrupt 0x19 (to inform the BIOS that the agent is a bootable device) in addition to registering as a BBS IPL device. The BIOS boot order CANNOT be changed in the Setup Menu.</p> <p>101b = Reserved for future use. If specified, treated as value 000b.</p> <p>110b = Reserved for future use. If specified, treated as value 000b.</p> <p>111b = Reserved for future use. If specified, treated as value 000b.</p>
7:6	Reserved	00b	Reserved, must be set to 00b.
5	DFU	0b	<p>Disable Flash Update</p> <p>If set to 1b, no updates to the Flash image using PROSet is allowed.</p> <p>The default for this bit is 0b; allow Flash image updates using PROSet.</p>
4	DLWS	0b	<p>Disable Legacy Wakeup Support</p> <p>If set to 1b, no changes to the Legacy OS Wakeup Support menu option is allowed.</p> <p>The default for this bit is 0b; allow Legacy OS Wakeup Support menu option changes.</p>



Bit	Name	Default	Description
3	DBS	0b	<p>Disable Boot Selection</p> <p>If set to 1b, no changes to the boot order menu option is allowed.</p> <p>The default for this bit is 0b; allow boot order menu option changes.</p>
2	DPS	0b	<p>Disable Protocol Select</p> <p>If set to 1b, no changes to the boot protocol is allowed.</p> <p>The default for this bit is 0b; allow changes to the boot protocol.</p>
1	DTM	0b	<p>Disable Title Message</p> <p>If set to 1b, the title message displaying the version of the boot agent is suppressed; the Control-S message is also suppressed. This is for OEMs who do not want the boot agent to display any messages at system boot.</p> <p>The default for this bit is 0b; allow the title message that displays the version of the boot agent and the Control-S message.</p>
0	DSM	0b	<p>Disable Setup Menu</p> <p>If set to 1b, no invoking the setup menu by pressing Control-S is allowed. In this case, the EEPROM can only be changed via an external program.</p> <p>The default for this bit is 0b; allow invoking the setup menu by pressing Control-S.</p>

### 10.3.2.1.3 Boot Agent Configuration Customization Options (Word 0x32)

Word 0x32 is used to store the version of the boot agent that is stored in the Flash image. When the Boot Agent loads, it can check this value to determine if any first-time configuration needs to be performed. The agent then updates this word with its version. Some diagnostic tools to report the version of the Boot Agent in the Flash also read this word. This word is only valid if the PPB is set to 0b. Otherwise the contents might be undefined.



**Table 10-1 Boot Agent Configuration Customization Options (Word 0x32)**

Bit	Name	Default	Description
15:12	MAJOR	0x1	PXE boot agent major version. The default for these bits is 0x1.
11:8	MINOR	0x2	PXE boot agent minor version. The default for these bits is 0x2.
7:0	BUILD	0x28	PXE boot agent build number. The default for these bits is 0x28.

### 10.3.2.1.4 IBA Capabilities (Word 0x33)

Word 0x33 is used to enumerate the boot technologies that have been programmed into the Flash. It is updated by IBA configuration tools and is not updated or read by IBA.

**Table 10-1 IBA Capabilities**

Bit	Name	Default	Description
15:14	SIG	01b	Signature These bits must be set to 01b to indicate that this word has been programmed by the agent or other configuration software.
13:5	Reserved	0x00	Reserved, must be set to 0x00.
4	iSCSI Boot Capability not present	0b	iSCSI boot capability not present (0b default).
3	EFI	0b	EFI EBC capability is present in Flash. 0b = The EFI code is not present (default). 1b = The EFI code is present.
2	Reserved	1b	Reserved, set to 1b.
1	UNDI	1b	PXE/UNDI capability is present in Flash. 1b = The PXE base code is present (default). 0b = The PXE base code is not present.
0	BC	1b	PXE base code is present in Flash. 0b = The PXE base code is not present. 1b = The PXE base code is present (default).





### 10.3.2.2 Checksum Word Calculation (Word 0x3F)

The Checksum word (Word 0x3F, NVM bytes 0x7E and 0x7F) is used to ensure that the base NVM image is a valid image. The value of this word should be calculated such that after adding all the words (0x00-0x3F) / bytes (0x00-0x7F), including the Checksum word itself, the sum should be 0xBABA. The initial value in the 16 bit summing register should be 0x0000 and the carry bit should be ignored after each addition.

**Note:** Hardware does not calculate the word 0x3F checksum during NVM write; it must be calculated by software independently and included in the NVM write data. Hardware does not compute a checksum over words 0x00-0x3F during NVM reads in order to determine validity of the NVM image; this field is provided strictly for software verification of NVM validity. All hardware configuration based on word 0x00-0x3F content is based on the validity of the Signature field of the NVM.

## 10.3.3 Basic Configuration Software Words

This section describes the meaningful NVM words in the basic configuration space that are used by software at word addresses 0x03-0x09.

### 10.3.3.1 Reserved (Word 0x03)

Bits	Name	Default	Description
15:12	Reserved	0x03	Reserved, set to 0x0.
11	LOM	1b	LOM Set to 1b.
10:0	Reserved	0x00	Reserved, set to 0x00.

**Note:** When software calculates the checksum, bit 1 of this word is set to 1b to indicate that the checksum is valid after the image is successfully programmed.

### 10.3.3.2 Reserved (Word 0x04)

Bits	Name	Default	Description
15:0	Reserved	0xFFFF	Reserved



### 10.3.3.3 Image Version Information (Word 0x05)

0x03 denotes tuning to support a design that includes a LAN switch. 0x04 denotes tuning for all other designs.

### 10.3.3.4 PBA Low and PBA High (Words 0x08 and 0x09)

Bits	Word	Default	Description
15:0	0x08	0xFFFF	PBA low.
15:0	0x09	0xFFFF	PBA high.

The nine-digit Printed Board Assembly (PBA) number used for Intel manufactured Network Interface Cards (NICs) and LAN on Motherboard (LOMs) are stored in a four-byte field. The dash itself is not stored, neither is the first digit of the 3-digit suffix, as it is always zero for the affected products. Note that through the course of hardware ECOs, the suffix field (byte 4) is incremented. The purpose of this information is to allow customer support (or any user) to identify the exact revision level of a product.

**Note:** Network driver software should not rely on this field to identify the product or its capabilities.

Example: PBA number = 123456-003 to Word 0x08 = 0x1234; Word 0x09 = 0x5603.

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## 11.0 Electrical and Timing Specifications

### 11.1 Introduction

This section describes the I219's recommended operating conditions, power delivery, DC electrical characteristics, power sequencing and reset requirements, PCIe specifications, reference clock, and packaging information.

### 11.2 Operating Conditions

#### 11.2.1 Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units
$T_{case}$	Case Temperature Under Bias	0	106	°C
$T_{storage}$	Storage Temperature Range	-40	125	°C
$V_i/V_o$	3.3 Vdc I/O Voltage	-0.3	3.7	Vdc
VCC	3.3 Vdc Periphery DC Supply Voltage	-0.3	3.7	Vdc
VCC0P9	Core Vdc Supply Voltage	-0.3	1.2	Vdc

**Notes:**

1. Ratings in this table are those beyond which permanent device damage is likely to occur. These values should not be used as the limits for normal device operation. Exposure to absolute maximum rating conditions for extended periods might affect device reliability.
2. Recommended operation conditions require accuracy of power supply of +/-5% relative to the nominal voltage.
3. Maximum ratings are referenced to ground (VSS).

#### 11.2.2 Recommended Operating Conditions

Symbol	Parameter	Min	Max	Units
$T_a$	Operating Temperature Range Commercial (Ambient; 0 CFS airflow)	0	85 <sup>1</sup>	°C

1. For normal device operation, adhere to the limits in this table. Sustained operations of a device at conditions exceeding these values, even if they are within the absolute maximum rating limits, can result in permanent device damage or impaired device reliability. Device functionality to stated Vdc and Vac limits is not guaranteed if conditions exceed recommended operating conditions.



## 11.3 Power Delivery

### 11.3.1 Voltage Regulator Power Supply Specifications

#### 11.3.1.1 3.3 Vdc Rail

Title	Description	Min	Max	Units
Rise Time	Time from 10% to 90% mark	0.1	100	ms
Monotonicity	Voltage dip allowed in ramp	N/A	0	mV
Slope	Ramp rate at any given time between 10% and 90% Min: $0.8 \cdot V(\text{min}) / \text{Rise time}(\text{max})$ Max: $0.8 \cdot V(\text{max}) / \text{Rise time}(\text{min})$	24	28800	V/s
Operational Range	Voltage range for normal operating conditions	3.13	3.46	V
Ripple	Maximum voltage ripple (peak to peak)	N/A	70	mV
Overshoot	Maximum overshoot allowed	N/A	100	mV

#### 11.3.1.2 Core Vdc Rail (External/Shared)

Title	Description	Min	Max	Units
Rise Time	Time from 10% to 90% mark	0.5	40	ms
Monotonicity	Voltage dip allowed in ramp	N/A	0	mV
Slope	Ramp rate at any given time between 10% and 90% Min: $0.8 \cdot V(\text{min}) / \text{Rise time}(\text{max})$ Max: $0.8 \cdot V(\text{max}) / \text{Rise time}(\text{min})$	7.6	8400	V/s
Operational Range	Voltage range for normal operating conditions	0.87	1.115	Vdc
Ripple	Maximum voltage ripple (peak to peak)	N/A	50	mV
Overshoot	Maximum overshoot allowed	N/A	100	mV
Decoupling Capacitance	Capacitance range	20	30	$\mu\text{F}$
Capacitance ESR	Equivalent series resistance of output capacitance	5	50	$\text{m}\Omega$



## 11.3.2 SVR Specification (Internal)

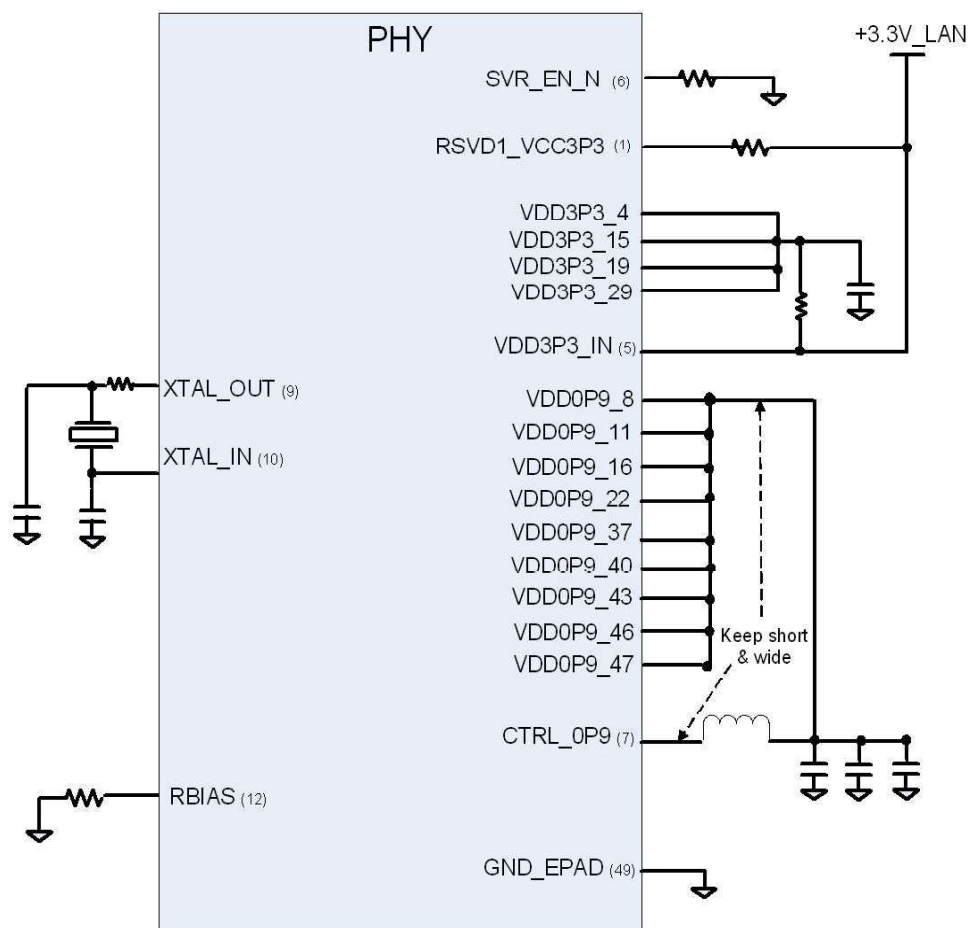
Parameter	Specifications			Units	Comments
	Min	Typ	Max		
Regulator Output Voltage ("Core" voltage)	0.8		1.2	Vdc	The default voltage is set to 0.93 Vdc
Output Voltage Accuracy	-3		+3	%	Not including line and load regulation errors.
Input Voltage Range	2.9	3.3	3.7	Vdc	Supply voltage range.
Load Current	0.01	0.3	0.5	A	Average value.
Output Voltage Under/Over Shoot	-10		+10	%	For min-to-max average load current change.
Transient Settling Time		100		μs	Duration of overshoot or undershoot.
Conversion Efficiency	80	85	90	%	
Switching Frequency		1.5625		MHz	
Output Filter Inductor	3.9	4.7		μH	
Output Filter Inductor DCR		0.1	0.318	Ω	+/-20%, values higher than the typical DCR value will lower the SVR conversion efficiency.
Output Filter Capacitor	20			μF	
Output Filter Capacitor ESR		5	50	mΩ	
Input Capacitor	22			μF	

## 11.3.3 Power On/Off Sequence

There is no power sequencing requirement for the I219.

## 11.3.4 Power Delivery Schematic Drawing

Figure 11-1 shows the power delivery schematic:



**Figure 11-1 Power Delivery Schematic**

**Table 11-1 Power Detection Threshold**

Symbol	Parameter	Specifications			Units
		Min	Typ	Max	
V1a	High-threshold for 3.3 Vdc supply	2.35	2.45	2.6	Vdc
V2a	Low-threshold for 3.3 Vdc supply	2.1	2.45	2.6	Vdc
V1b	High-threshold for Core Vdc supply	0.6	0.75	0.85	Vdc
V2b	Low-threshold for Core Vdc supply	0.45	0.65	0.75	Vdc



## 11.4 I/O DC Parameter

### 11.4.1 3.3 Vdc I/O (Open Drain)

Parameter	Minimum	Typical	Maximum	Unit
VIL	-0.4	0	0.8	Vdc
VIH	2	3.3	3.6	Vdc
VOL	-0.4	0	0.4	Vdc
VOH	2.4	3.3	3.6	Vdc
I <sub>pullup</sub>	30	50	75	μA
I <sub>leakage</sub>			10	μA
Ci		2	4	pF

Pin Name	Bus Size	Description
CLK_REQ_N	1	Open-drain I/O.
SMB_CLK	1	Open-drain I(H)/O with snap back NMOS ESD cell.
SMB_DATA	1	Open-drain I(H)/O with snap back NMOS ESD cell.

**Note:** SMBus leakage current when the I219 is off is <10 μA.

### 11.4.2 3.3 Vdc I/O

Parameter	Conditions	Minimum	Typical	Maximum	Units
VIL		-0.3	0	0.4	Vdc
VIH		2	3.3	3.6	Vdc
VOL	I <sub>OL</sub> = 9 mA VCC = Min	-0.4	0	0.4	Vdc
VOH	I <sub>OH</sub> = -9 mA VCC = Min	2	2.6	2.8	Vdc
I <sub>pullup</sub>		30	50	75	μA
I <sub>leakage</sub>		15 (pull-down)	25 (pull-down)	35 (pull-down)	μA
Ci			2	4	pF
PU			50		KΩ
PD			50		KΩ



Pin Name	Bus Size	Description
RSVD1_VCC3P3 RSVD2_VCC3P3	2	I/O, PU
LED0 LED1 LED2	3	I/O, PU
JTAG_TDI	1	I/O, PU
JTAG_TMS	1	I/O, PU
JTAG_TDO	1	I/O, PU
JTAG_TCK	1	I/O, PU

### 11.4.3 Input Buffer Only

Parameter	Conditions	Minimum	Typical	Maximum	Units
VIL		-0.3	0	0.8	Vdc
VIH		2	3.3	3.6	Vdc
I <sub>pullup</sub>		30	50	75	μA
I <sub>leakage</sub>				10	μA
CI			2	4	pF

Pin Name	Bus Size	Description
LAN_DISABLE_N	1	I(H), PU
TEST_EN	1	I (no PU, no PD)
PE_RST_N	1	I(H), PU

### 11.4.4 PCIe DC/AC Specifications

#### 11.4.4.1 PCIe Specifications (Transmitter)

**Note:** Refer to the I219 PCIe-Based Test Procedure for more details.

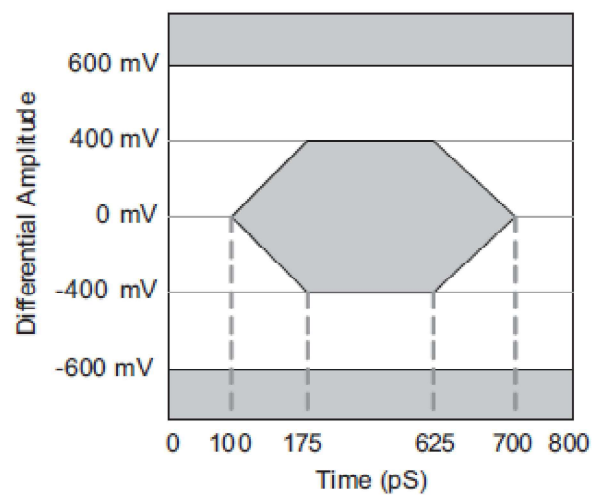
Symbol	Parameter	1.25 GT/s		Units	Comments
		Min	Max		
UI	Unit interval.	799.92	800.08	ps	Each UI is 800 ps +/- 100 ppm.
V <sub>tx-diff-pp</sub>	Differential peak-to-peak Tx voltage swing.	0.8	1.2	Vdc	
T <sub>tx-eye</sub>	Transmitter eye including all jitter sources.	0.75		UI	
T <sub>tx-eye-median-to-max-jitter</sub>	Maximum time between the jitter median and maximum deviation from the median.		0.125	UI	





Symbol	Parameter	1.25 GT/s		Units	Comments
		Min	Max		
$RL_{tx-diff}$	Tx package plus silicon differential return loss.	7		db	
$RL_{tx-cm}$	Tx package plus silicon common mode return loss.	6		db	
$Z_{tx-diff-dc}$	DC differential Tx impedance.	75	120	$\Omega$	
$V_{tx-cm-ac-p}$	Tx V ac common mode voltage (2.5 GT/s).		20	mV	
$I_{tx-short}$	Transmitter short-circuit current limit.		90	mA	
$V_{tx-dc-cm}$	Transmitter DC common mode voltage.	0	3.6	Vdc	
$V_{tx-cm-dc-active-idle-delta}$	Absolute delta of DC common mode voltage during L0 and electrical idle.	0	100	mV	
$V_{tx-cm-dc-line-delta}$	Absolute delta of DC common mode voltage between D+ and D-.	0	25	mV	
$V_{tx-idle-diff-ac-p}$	Electrical idle differential peak output voltage.	0	20	mV	
$T_{tx-idle-set-to-idle}$	Maximum time to transition to a valid electrical idle after sending an EIOS.		35	ns	
$T_{tx-idle-to-diff-data}$	Maximum time to transition to valid differential signaling after leaving electrical idle.		35	ns	

**Note:** Figure 11-2 is for informational purposes only. Do not use for actual eye comparisons.



Note: Not To Scale

**Figure 11-2 Transmitter Eye Diagram**

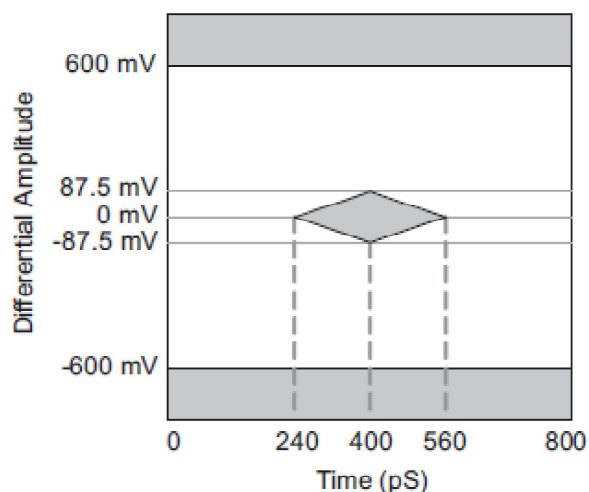


## 11.4.4.2 PCIe Specifications (Receiver)

Symbol	Parameter	1.25 GT/s		Units	Comments
		Min	Max		
UI	Unit interval.	799.92	800.08	ps	Each UI is 800 ps +/- 100 ppm
$V_{rx-diff-pp-cc}$	Differential peak-to-peak Rx voltage swing for common clock.	0.175	1.2	Vdc	
$V_{rx-diff-pp-dc}$	Differential peak-to-peak Rx voltage swing for data clock.	0.175	1.2	Vdc	
$T_{rx-eye}$	Receiver minimum eye time opening.	0.4	N/A	UI	
$T_{rx-eye-median2maxjitter}$	Maximum time delta between median and deviation from median.	N/A	0.3	UI	
$RL_{rx-diff}$	Rx differential return loss.	6	N/A	dB	
$RL_{rx-cm}$	Rx CM return loss.	5	N/A	dB	
$Z_{rx-diff-dc}$	Rx differential Vdc impedance.	80	120	$\Omega$	
$V_{rx-cm-ac-p}$	Rx Vac CM voltage.	N/A	150	mVp	
$Z_{rx-high-imp-dc-pos}$	DC input CM impedance for $V > 0$ .	50 K	N/A	$\Omega$	
$Z_{rx-high-imp-dc-neg}$	DC input CM impedance for $V < 0$ .	1 K	N/A	$\Omega$	
$V_{rx-idle-det-diff-p-p}$	Electrical idle detect threshold.	65	175	mV	

**Note:** The I219 has integrated PCIe termination that results in attenuating the voltage swing of the PCIe clock supplied by Cougar Point. This is in compliance with the PCIe CEM 1.1 specification. More detail is available in the *Cougar Point PDG*.

**Note:** Figure 11-3 is intended to show the difference between the PCIe 1.0 and PCIe-based receiver sensitivity templates. It is for informational purposes only.



**Figure 11-3 Receiver Eye Diagram**



### 11.4.4.3 PCIe Clock Specifications

The PCIe clock specification can be found in the *PCI Express Card Electromechanical Specification 1.1*, section 2.1.

## 11.5 Discrete/Integrated Magnetics Specifications

Criteria	Condition	Values (Min/Max)
Voltage Isolation	At 50 to 60 Hz for 60 seconds	1500 Vrms (min)
	For 60 seconds	2250 Vdc (min)
Open Circuit Inductance (OCL) or OCL (alternate)	With 8 mA DC bias at 25 °C	400 $\mu$ H (min)
	With 8 mA DC bias at 0 °C to 70 °C	350 $\mu$ H (min)
Insertion Loss	100 kHz through 999 kHz 1.0 MHz through 60 MHz 60.1 MHz through 80 MHz 80.1 MHz through 100 MHz 100.1 MHz through 125 MHz	1 dB (max) 0.6 dB (max) 0.8 dB (max) 1.0 dB (max) 2.4 dB (max)
Return Loss	1.0 MHz through 40 MHz 40.1 MHz through 100 MHz When reference impedance is 85 $\Omega$ , 100 $\Omega$ , and 115 $\Omega$ Note that return loss values might vary with MDI trace lengths. The LAN magnetics might need to be measured in the platform where it is used.	18 dB (min) 12 to 20 * LOG (frequency in MHz / 80) dB (min)
Crosstalk Isolation Discrete Modules	1.0 MHz through 29.9 MHz 30 MHz through 250 MHz 250.1 MHz through 375 MHz	-50.3+(8.8*(freq in MHz / 30)) dB (max) -26-(16.8*(LOG(freq in MHz / 250))) dB (max) -26 dB (max)
Crosstalk Isolation Integrated Modules	1.0 MHz through 10 MHz 10.1 MHz through 100 MHz 100.1 MHz through 375 MHz	-50.8+(8.8*(freq in MHz / 10)) dB (max) -26-(16.8*(LOG(freq in MHz / 100))) dB (max) -26 dB (max)
Diff to CMR	1.0 MHz through 29.9 MHz 30 MHz through 500 MHz	-40.2+(5.3*((freq in MHz / 30)) dB (max) -22-(14*(LOG((freq in MHz / 250)))) dB (max)
CM to CMR	1.0 MHz through 270 MHz 270.1 MHz through 300 MHz 300.1 MHz through 500 MHz	-57+(38*((freq in MHz / 270)) dB (max) -17-2*((300-(freq in MHz) / 30) dB (max) -17 dB (max)

## 11.6 Mechanical

Body Size (mm)	Ball Count	Ball Pitch	Ball Matrix	Center Matrix	Substrate
6x6 mm	48	0.4 mm	N/A, Peripheral	N/A, Exposed Pad	N/A Lead Frame-Based Package



## 11.7 Oscillator/Crystal Specifications

Table 11-2 lists required parameters.

**Table 11-2 External Crystal Specifications**

Parameter Name	Symbol	Recommended Value	Max/Min Range	Conditions
Frequency	$f_o$	25 [MHz]		@25 [°C]
Vibration Mode		Fundamental		
Frequency Tolerance @25 °C	$Df/f_o$ @25 °C	±30 [ppm]		@25 [°C]
Temperature Tolerance	$Df/f_o$	±30 [ppm]		0 to +70 [°C]
Series Resistance (ESR)	$R_s$		50 [Ω] max	@25 [MHz]
Crystal Load Capacitance	$C_{load}$	18 [pF]		
Shunt Capacitance	$C_o$		6 [pF] max	
Drive Level	$D_L$		200 [μW] max	
Aging	$Df/f_o$	±5 ppm per year	±5 ppm per year max	
Calibration Mode		Parallel		
Insulation Resistance			500 [MΩ] min	@ 100 Vdc

Crystal must meet or exceed the specified drive Level (DL). Refer to the crystal design guidelines in the *Intel® 5 Series Family PDG*.

**Table 11-3 Clock Oscillator Specifications**

Parameter Name	Symbol/Parameter	Conditions	Min	Typ	Max	Unit
Frequency	$f_o$	@25 [°C]		25.0		MHz
Clock Amplitude	Vmax		0.8		1.8	Vdc
Clock Amplitude	Vmin				0	Vdc
Frequency Tolerance	$f/f_o$	20 to +70		±50		[ppm]
Operating Temperature	$T_{opr}$	-20 to +70				°C
Aging	$f/f_o$			±5 ppm per year		[ppm]
TH_XTAL_IN	XTAL_IN High Time		13	20		ns
TL_XTAL_IN	XTAL_IN Low Time		13	20		ns
TR_XTAL_IN	XTAL_IN Rise	10% to 90%			5	ns
TF_XTAL_IN	XTAL_IN Fall	10% to 90%			5	ns
TJ_XTAL_IN	XTAL_IN Total Jitter				200 <sup>1</sup>	ps

1. Broadband peak-to-peak = 200 ps, Broadband rms = 3 ps, 12 KHz to 20 MHz rms = 1 ps



### XTAL\_IN/XTAL\_OUT Timing

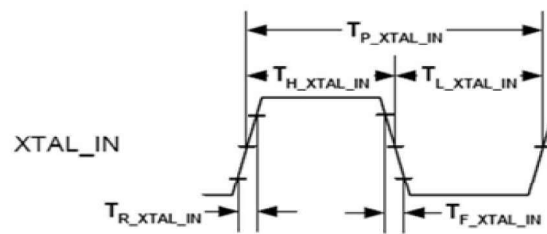
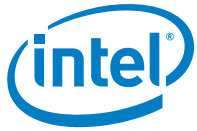


Figure 11-4 XTAL Timing Diagram



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## 12.0 Mobile Design Considerations and Guidelines

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The PCH incorporates an integrated 10/100/1000 Mb/s MAC controller that can be used with an external Intel® Ethernet Connection I219 (PHY) shown in [Figure 12-1](#). Its bus master capabilities enable the component to process high-level commands and perform multiple operations, which lowers processor use by offloading communication tasks from the processor.

The PCH, which hereinafter refers to the integrated MAC within the PCH, supports the SMBus interface for manageability while in an Sx state and PCI Express\* (PCIe\*) for 10/100/1000 Mb/s traffic in an S0 state.

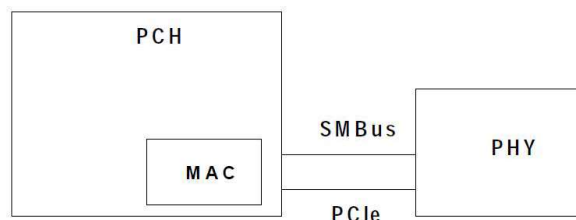
**Note:** The PCIe interface is not PCIe-compliant. It operates at half of the PCI Express\* (PCIe\*) Specification v1.0 (2.5 GT/s) speed. In this section, the term “PCIe-based” is interchangeable with “PCIe.” There are no design layout differences between normal PCIe and the PCIe-based interface.

The PHY interfaces with the integrated MAC through two interfaces: PCIe and SMBus. In SMBus mode, the link speed is reduced to 10 Mb/s. The PCIe interface incorporates two aspects: a PCIe-based SerDes (electrically) and a custom logic protocol for messaging between the integrated MAC and the PHY.

**Note:** Gigabit Ethernet requires an SPI Flash to host firmware and does not work without an SPI Flash on board.

The integrated MAC supports multi-speed operation (10/100/1000 Mb/s). The integrated MAC also operates in full-duplex at all supported speeds or half-duplex at 10/100 Mb/s as well as adhering to the IEEE 802.3x Flow Control Specification.

**Note:** References to the AUX power rail means the power rail is available in all power states including G3 to S5 transitions and Sx states with Wake on LAN (WoL) enabled. For example, V3P3\_AUX in this section refers to a rail that is powered under the conditions previously mentioned.



**Figure 12-1 PCH/PHY Interface Connections**

**Table 12-1 SMBus Data Signals on the PCH**

Group	PHY Signal Name	PCH Signal Name	Description
Data	SMB_DATA	SMLINK0_DATA	SMBus data

**Table 12-2 PCIe Data Signals on the PCH**

Group	PHY Signal Name	PCH Signal Name	Description
Data	PETp PETn	PETp PETn	PCIe transmit pair
Data	PERp PERn	PERp PERn	PCIe receive pair

**Note:** The appropriate NVM descriptor soft strap (PCHSTRP9) should define which PCIe port is configured as GbE LAN. Refer to the PCH EDS document for the specific ports that can be used for GbE LAN.

**Table 12-3 PCIe Data Signals on the PCH**

Group	PHY Signal Name	PCH Signal Name	Description
Clock	SMB_CLK	SML0_CLK	SMBus clock.
Clock	PE_CLKP PE_CLKN	CLKOUT_PCIE[7:0]_P <sup>1</sup> CLKOUT_PCIE[7:0]_N <sup>1</sup>	PCIe clock.
Clock	CLK_REQ_N	PCIECLKRQ[7:0]#	PCIe clock request.
Reset	PE_RST_N	PLTRST#	PCIe reset.

1. These signals come from the PCH and drive the PHY.

## 12.1 I219 Overview

The Intel® Ethernet Connection I219 is a single port compact component designed for 10/100/1000 Mb/s operation. It enables a single port Gigabit Ethernet (GbE) implementation in a very small area, easing routing constraints from the PCH chipset to the PHY.

The PHY provides a standard IEEE 802.3 Ethernet interface for 1000BASE-T, 100BASETX, and 10BASE-T applications (802.3ab, 802.3u, and 802.3i, respectively).

### 12.1.1 I219 Interconnects

The main interfaces for the I219 are PCIe and SMBus on the host side and Media Dependent Interface (MDI) on the link side. Transmit traffic is received from the PCH as either PCIe or SMBus packets on the host interconnect and transmitted as Ethernet packets on the MDI link. Receive traffic arrives as Ethernet packets on the MDI link and is transferred to the PCH through either the PCIe or SMBus interconnects.

The PHY switches the in-band traffic automatically between PCIe and SMBus based on platform reset. The transition protocol is done through SMBus. The PCIe interface is powered down when the Ethernet link is running in an Sx state.





## 12.1.2 PCIe-Based Interface

A high-speed SerDes interface uses PCIe electrical signaling at half speed while utilizing a custom logical protocol for active state operation mode.

**Note:** PCIe validation tools cannot be used for electrical validation of this interface. However, PCIe layout rules apply for on-board routing.

### 12.1.2.1 PCIe Interface Signals

The signals used to connect between the PCH and the PHY in this mode are:

- Serial differential pair running at 1.25 Gb/s for Rx.
- Serial differential pair running at 1.25 Gb/s for Tx.
- 100-MHz differential clock input to the PHY is generated by the PCH.
- Power and clock good indication to the PHY PE\_RST\_N.
- Clock control through CLK\_REQ\_N (see [Table 12-3](#)). This PHY output should be tied to the PCH input and pulled up with a 10 K $\Omega$  resistor connected to 3.3 V DC AUX power (present in G3 to S5).

### 12.1.2.2 PCIe Operation and Channel Behavior

The I219 runs only at 1250 Mb/s speed; 1/2 the Gen 1, 2.5 Gb/s PCIe frequency. Each PCIe root port in the PCH has the ability to run at 1250 Mb/s. The configuration for a PCH PCIe port attached to a PCIe Intel PHY device is preloaded from the GbE region of the NVM. The selected port adjusts the transmitter to run at 1/2 the Gen 1 PCIe speed, and does not need to be PCIe compliant.

Packets transmitted and received over the PCIe interface are full Ethernet packets and not PCIe transaction/link/physical layer packets.

### 12.1.2.3 PCIe Connectivity

The PHY transmit/receive pins are output/input signals and are connected to the PCH as listed in [Table 12-1](#) through [Table 12-3](#).

### 12.1.2.4 PCIe Reference Clock

The PCIe Interface uses a 100-MHz differential reference clock, denoted PE\_CLKP and PE\_CLKN. This signal is typically generated on the platform and routed to the PCIe port.

The frequency tolerance for the PCIe reference clock is  $\pm 300$  ppm.



## 12.1.3 SMBus Interface

SMBus is a low speed (100/400/1000 KHz) serial bus used to connect various components in a system. SMBus is used as an interface to pass traffic between the PHY and the PCH when the platform is in a low power state (Sx). The interface is also used to enable the PCH to configure the PHY as well as pass in-band information between them.

The SMBus uses two primary signals to communicate: SMBCLK and SMBDATA. Both of these signals float high with board-level  $499\ \Omega \pm 5\%$  pull-up resistors.

### 12.1.3.1 SMBus Connectivity

Table 12-1 through Table 12-3 list the relationship between PHY SMBus pins to the PCH LAN SMBus pins.

**Note:** The SMBus signals (SMB\_DATA and SMB\_CLK) cannot be connected to any other devices other than the integrated MAC. Connect the SMB\_DATA and SMB\_CLK pins to the integrated MAC SML0DATA and SML0CLK pins, respectively.

## 12.1.4 PCIe and SMBus Modes

In GbE operation, PCIe is used to transmit and receive data and for MDIO status and control. The PHY automatically switches the in-band traffic between PCIe and SMBus based on the platform power state. Table 12-4 lists the operating modes of PCIe and SMBus.

The I219 automatically switches the in-band traffic between PCIe and SMBus based on the system power state.

**Table 12-4** PCIe and SMBus Operating Modes

System/Intel Management Engine State	PHY	
	SMBus	PCIe
S0 and PHY Power Down	Not used	Electrical Idle (EI)
S0 and Idle or Link Disconnect	Not used	EI
S0 and Link in Low Power Idle (LPI)	Not used	EI
S0 and active	Not used	Active
Sx	Active	Power down
Sx and DMoff	Active	Power down



## 12.1.5 Transitions Between PCIe and SMBus Interfaces

### 12.1.5.1 Switching from SMBus to PCIe

Communication between the integrated MAC and the PHY is done through the SMBus each time the system is in a low power state (Sx). The integrated MAC/PHY interface is needed while the Manageability Engine (ME) is still active to transfer traffic, configuration, control and status or to enable host wake up from the PHY.

Possible states for activity over the SMBus:

1. After power on (G3 to S5).
2. On system standby (Sx).

The switching from the SMBus to PCIe is done when the PE\_RST\_N signal goes high.

- Any transmit/receive packet that is not completed when PE\_RST\_N is asserted is discarded.
- Any in-band message that was sent over the SMBus and was not acknowledged is re-transmitted over PCIe.

### 12.1.5.2 Switching from PCIe to SMBus

The communication between the integrated MAC and the PHY is done through PCIe each time the platform is in active power state (S0). Switching the communication to SMBus is only needed for ME activity or to enable host wake up in low power states and is controlled by the ME.

The switching from PCIe to SMBus is done when the PE\_RST\_N signal goes low.

- Any transmit/receive packet that is not completed when PE\_RST\_N goes to 0b is discarded.
- Any in-band message that was sent over PCIe and was not acknowledged is re-transmitted over SMBus.

## 12.2 Platform LAN Design Guidelines

These sections provide recommendations for selecting components and connecting special pins. For GbE designs, the main elements are:

- The PCH chipset.
- The Intel® Ethernet Connection I219.
- A magnetics module and RJ-45 connector
- A GbE region NVM (Non Volatile Memory) image
- A clock source.



## 12.2.1 General Design Considerations for the Intel® Ethernet Connection I219

Sound engineering practices must be followed with respect to unused inputs by terminating them with pull-up or pull-down resistors, unless otherwise specified in a datasheet, design guide or reference schematic. Pull-up or pull-down resistors must not be attached to any balls identified as “No Connect.” These devices might have special test modes that could be entered unintentionally.

**Note:** The suggested parts recommended in this section (magnetics, crystals, oscillators, etc.) are either in evaluation or have been used successfully in previous designs with good results. Intel recommends that all selected parts must be validated on each production design.

### 12.2.1.1 Clock Source

All designs require a 25-MHz clock source. The PHY uses the 25-MHz source to generate clocks up to 125 MHz and 1.25 GHz for both the PHY circuits and the PCIe interface. For optimum results with lowest cost, a 25-MHz parallel resonant crystal can be used along with the appropriate load capacitors at the XTAL\_OUT (X2) and XTAL\_IN (X1) leads. The frequency tolerance of the timing device should equal 30 ppm or better. Further detail is found in [Section 12.19](#) and [Section 12.20.15](#).

**Note:** XTAL\_OUT and XTAL\_IN are the signal names for the PHY.

There are three steps to crystal qualification:

1. Verify that the vendor’s published specifications in the component datasheet meet the required conditions for frequency, frequency tolerance, temperature, oscillation mode and load capacitance as specified in the respective datasheet.
2. Perform physical layer conformance testing and EMC (FCC and EN) testing in real systems.
3. Independently measure the component’s electrical parameters in real systems. Measure frequency at a test output to avoid test probe loading effects at the PHY. Check that the measured behavior is consistent from sample to sample and that measurements meet the published specifications. For crystals, it is also important to examine startup behavior while varying system voltage and temperature.

### 12.2.1.2 Magnetics Module

The magnetics module has a critical effect on overall IEEE and emissions conformance. The device should meet the performance required for a design with reasonable margin to allow for manufacturing variation. Carefully qualifying new magnetics modules prevents problems that might arise because of interactions with other components or the printed circuit board itself.

The steps involved in magnetics module qualification are similar to those for crystal qualification:

1. Verify that the vendor’s published specifications in the component datasheet meet or exceed the required IEEE specifications.
2. Independently measure the component’s electrical parameters on the test bench, checking samples from multiple lots. Check that the measured behavior is consistent from sample to sample and that measurements meet the published specifications.
3. Perform physical layer conformance testing and EMC (FCC and EN) testing in real systems. Vary temperature and voltage while performing system-level tests.



Magnetics modules for 1000BASE-T Ethernet as used by the PHY only are similar to those designed solely for 10/100 Mb/s, except that there are four differential signal pairs instead of two. The following magnetics modules are not recommended, however, they have been used successfully in previous designs:

**Table 12-5 Discrete Magnetics Modules: Manufacturers and Part Numbers**

Manufacturer	Part Number	Notes
Pulse*	H5120	16.51 x 9.65 x 2.08 mm, 8 core
Bothhand*	GST5009LF	15.10 x 10 x 4 mm, 8 core
Delta*	LFE9249-R-IN	15.10 x 10 x 4 mm, 8 core

**Table 12-6 Discrete RJ45**

Manufacturer	Part Number	Notes
Lotes*	AJKM0007-P001A01	Thinnest solution, 5.2 mm height
Foxconn	JM3611-NS420013-7H	Low profile, 10 mm height
Pulse	E6688-001-01-L	Low profile, 10 mm height

### 12.2.1.3 Criteria for Integrated Magnetics Electrical Qualification

Table 12-7 gives the criteria used to qualify integrated magnetics.

**Table 12-7 Integrated Magnetics Recommended Qualification Criteria**

Open Circuit Inductance (OCL)	w/8 mA DC bias; at 25 °C	400 $\mu$ H Min
	w/8 mA DC bias; at 0 °C to 70 °C	350 $\mu$ H Min
Insertion Loss	100 KHz through 999 KHz 1.0 MHz through 60.0 MHz 60.1 MHz through 80.0 MHz 80.1 MHz through 100.0 MHz 100.1 MHz through 125.0 MHz	1dB Max 0.6dB Max 0.8dB Max 1.0dB Max 2.4dB Max
Return Loss	1.0 MHz through 40.0 MHz 40.1 MHz through 100.0 MHz When reference impedance is 85 Ohms, 100 Ohms, and 115 Ohms, Note that R.L. values may vary with MDI trace lengths. The LAN magnetics may need to be measured in the platform where it will be used.	18.0 dB Min $12 - 20 * \text{LOG} (\text{Freq in MHz} / 80) \text{ dB Min}$
Crosstalk Isolation Discrete Modules	1.0 MHz through 29.9 MHz 30.0 MHz through 250.0 MHz 250.1 MHz through 375.0 MHz	$-50.3 + (8.8 * (\text{Freq in MHz} / 30)) \text{ dB Max}$ $-(26 - (16.8 * (\text{LOG}(\text{Freq in MHz} / 250 \text{ MHz})))) \text{ dB Max}$ -26.0 dB Max
Crosstalk Isolation Integrated Modules (Proposed)	1.0 MHz through 10 MHz 10.0 MHz through 100.0 MHz 100 MHz through 375.0 MHz	$-50.8 + (8.8 * (\text{Freq in MHz} / 10)) \text{ dB Max}$ $-(26 - (16.8 * (\text{LOG}(\text{Freq in MHz} / 100 \text{ MHz})))) \text{ dB Max}$ -26.0 dB Max



**Table 12-7 Integrated Magnetics Recommended Qualification Criteria**

<b>Diff to CMR</b>	1 MHz through 29.9 MHz 30.0 MHz through 500 MHz	$-40.2 + (5.3 * ((\text{Freq in MHz} / 30)))$ dB Max $-(22 - (14 * (\text{LOG}((\text{Freq in MHz} / 250))))$ dB Max
<b>CM to CMR</b>	1 MHz through 270 MHz 270.1 MHz through 300 MHz 300.1 MHz through 500 MHz	$-57 + (38 * ((\text{Freq in MHz} / 270)))$ dB Max $-17 - 2 * ((300 - (\text{Freq in MHz} / 30))$ dB Max -17 dB Max
<b>Hi-Voltage Isolation</b>	1500 Vrms at 50 or 60 Hz for 60 sec. or: 2250 Vdc for 60 seconds	Minimum

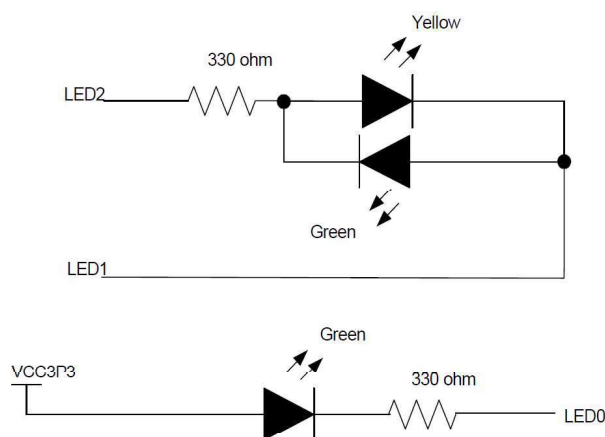
## 12.2.2 NVM for PHY Implementations

The LAN only supports an SPI Flash, which is connected to the PCH. Several words of the NVM are accessed automatically by the device after reset to provide pre-boot configuration data before it is accessed by host software. The remainder of the NVM space is available to software for storing the MAC address, serial numbers, and additional information. More details may be obtained from the Datasheet.

Intel has an MS-DOS\* software utility called EUpdate that is used to program the SPI Flash images in development or production line environments. A copy of this program can be obtained through your Intel Field Service representative.

## 12.2.3 LED

The PHY has three LED outputs that can be configured via the NVM. The hardware configuration is shown in Figure 12-2.



**Figure 12-2 LED Hardware Configuration**

**Note:** Intel recommends that the LED pins only be used to drive LEDs. These pins tri-state in ULP mode and might not drive valid logic levels.

Refer to the *Intel® Ethernet Connection I219 Reference Schematic* for default LED color based on reference design.



Refer to [Section 9.0](#) of this datasheet for details regarding the programming of the LED's and the various modes. The default values for the PHY (based on the LED NVM setting--word 0x18 of the LAN region) are listed in the [Table 12-8](#).

**Table 12-8 LED Default Values**

LED	Mode	Color	Blink	Polarity
LED0	Link Up/Activity	Green	200 ms on/200 ms off	Active low
LED1	Link 1000	Yellow	No	Active low
LED2	Link 100	Green	No	Active low

### 12.2.3.1 RBIAS

RBIAS requires external resistor connection to bias the internal analog section of the device. The input is sensitive to the resistor value. Resistors of 1% tolerance must be used. Connect RBIAS through a 3.01 K $\Omega$  1% pull-down resistor to ground, then place it no more than one half inch (0.5") away from the PHY.

### 12.2.3.2 LAN Disable

The PHY enters a power-down state when the LAN\_DISABLE\_N pin is asserted low. Exiting this mode requires setting the LAN\_DISABLE\_N pin to a logic one. Connect LAN\_DISABLE\_N to LAN\_PHY\_PWR\_CTRL / GPIO12 on the PCH.

## 12.2.4 Exposed Pad\* (e-Pad) Design and SMT Assembly Guide

### 12.2.4.1 Overview

This section provides general information about ePAD and SMT assemblies. Chip packages have exposed die pads on the bottom of each package to provide electrical interconnections with the printed circuit board. These ePADs also provide excellent thermal performance through efficient heat paths to the PCB.

Packages with ePADs are very popular due to their low cost. Note that this section provides only basic information and references in regards to the ePAD. It is recommended that each customer consult their fab and assembly house to obtain more details on how to implement the ePAD package design. Each fab and assembly house might need to tune the land pattern/stencil and create a solution that best suits their methodology and process.

## 12.2.4.2 PCB Design Requirements

To maximize both heat removal and electrical performance, a land pattern must be incorporated on the PCB within the footprint of the package corresponding to the exposed metal pad or exposed heat slug of the package as shown in the following figures. Refer to the specific product datasheet for actual dimensions.

**Note:** Due to the package size, a via-in-pad configuration must be used. Figure 12-3 and Figure 12-4 are general guidelines. See Figure 12-5 for specific via-in-pad thermal pattern recommendations.

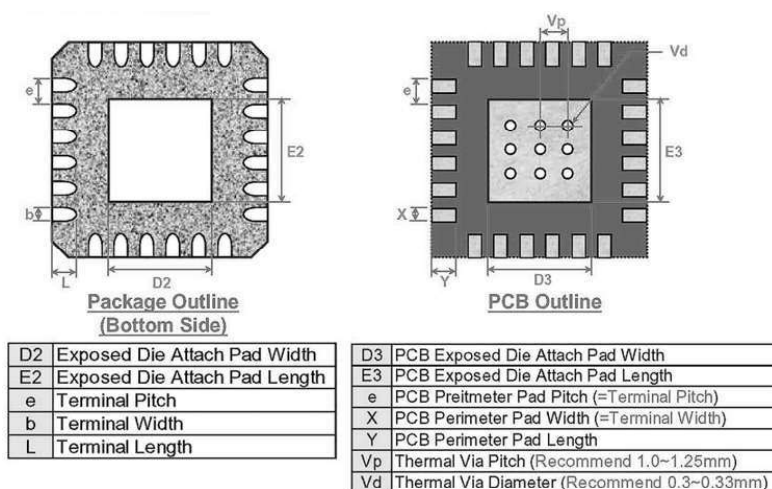


Figure 12-3 Typical ePAD Land Pattern

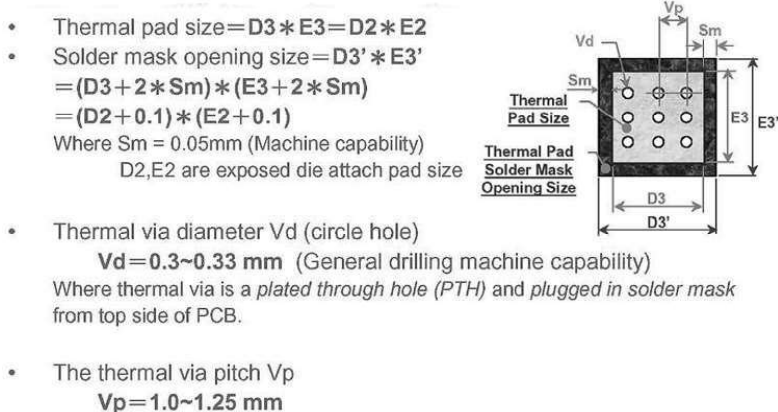


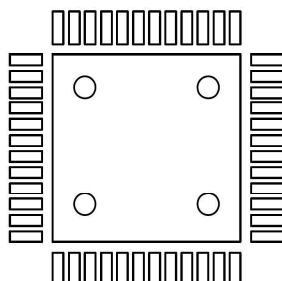
Figure 12-4 Typical Thermal Pad and Via Recommendations

**Note:** Encroached and uncapped via configurations have voids less than the maximum allowable void percentage. Uncapped via provides a path for trapped air to escape during the reflow soldering process.





**Note:** Secondary side solder bumps might be seen in an uncapped via design. This needs to be considered when placing components on the opposite side of the PHY.



**Figure 12-5 Recommended Thermal Via Patterns**

### 12.2.4.3 Board Mounting Guidelines

The following are general recommendations for mounting a QFN-48 device on the PCB. This should serve as the starting point in assembly process development and it is recommended that the process should be developed based on past experience in mounting standard, non-thermally/electrically enhanced packages.

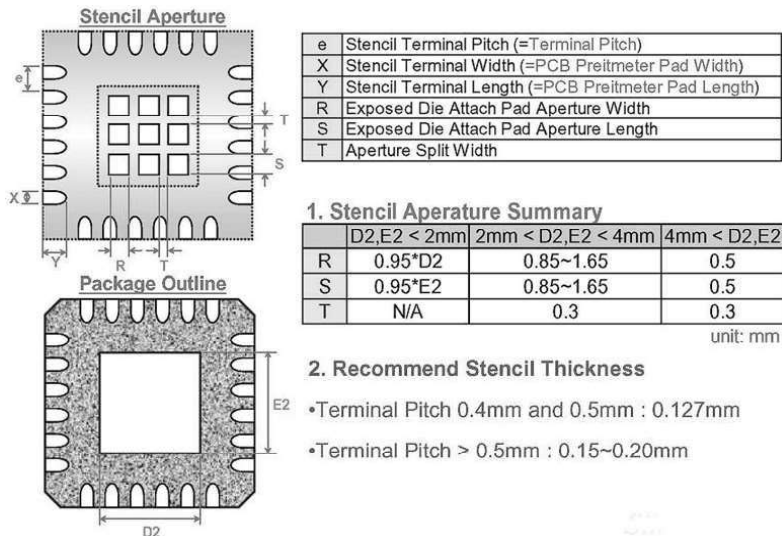
### 12.2.4.4 Stencil Design

For maximum thermal/electrical performance, it is required that the exposed pad/slug on the package be soldered to the land pattern on the PCB. This can be achieved by applying solder paste on both the pattern for lead attachment as well as on the land pattern for the exposed pad. While for standard (non-thermally/non-electrically enhanced) lead-frame based packages the stencil thickness depends on the lead pitch and package co-planarity, the package standoff must also be considered for the thermally/electrically enhanced packages to determine the stencil thickness. In this case, a stencil foil thickness in the range of 5-6 mils (or 0.127—0.152 mm) is recommended; likely or practically, a choice of either 5 mils or 6 mils. Tolerance-wise, it should not be worse than  $\pm 0.5$  mil.

**Note:** Industry specialists typically use  $\pm 0.1$  mil tolerance on stencil for its feasible precision.

The aperture openings should be the same as the solder mask openings on the land pattern. Since a large stencil opening may result in poor release, the aperture opening should be subdivided into an array of smaller openings, similar to the thermal land pattern shown in [Figure 12-6](#).

**Note:** Refer to the specific product datasheet for actual dimensions.



**Figure 12-6 Stencil Design Recommendation**

Important General Guidelines:

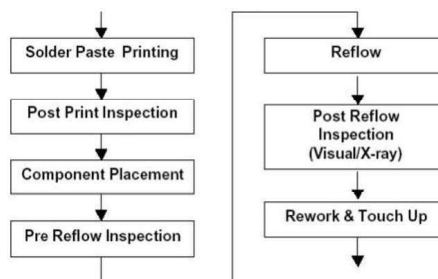
- The Stencil Aperture Openings of the e-PAD must not go outside of the exposed landing area (solder mask opening).
- The Stencil Aperture Openings of the e-PAD should be about 80% of the exposed landing area (solder mask opening).

The I219 e-PAD has D2=E2=3 mm. Therefore, the Stencil Design can only have four aperture openings for the e-PAD. This can be achieved by setting R=S=1.35 mm and T=0.3. Using this arrangement, the Aperture's/e-PAD area is 81% of the exposed landing area (solder mask opening).

**Note:** This information is intended only as general guidance. Consult with the manufacturer to confirm the final design meets requirements.

## 12.2.4.5 Assembly Process Flow

Figure 12-7 below shows the typical process flow for mounting packages to the PCB.

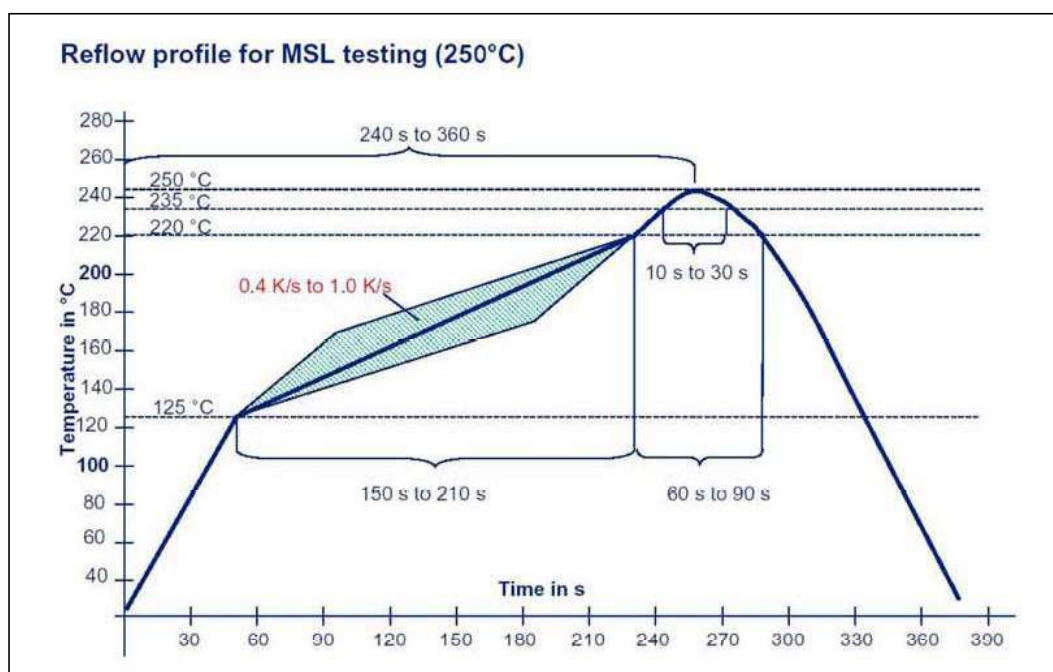


**Figure 12-7 Assembly Flow**



## 12.2.4.6 Reflow Guidelines

The typical reflow profile consists of four sections. In the preheat section, the PCB assembly should be preheated at the rate of 1 to 2 °C/sec to start the solvent evaporation and to avoid thermal shock. The assembly should then be thermally soaked for 60 to 120 seconds to remove solder paste volatiles and for activation of flux. The reflow section of the profile, the time above liquidus should be between 45 to 60 seconds with a peak temperature in the range of 245 to 250 °C, and the duration at the peak should not exceed 30 seconds. Finally, the assembly should undergo cool down in the fourth section of the profile. A typical profile band is provided in Figure 12-8, in which 220 °C is referred to as an approximation of the liquidus point. The actual profile parameters depend upon the solder paste used and specific recommendations from the solder paste manufacturers should be followed.



### Notes:

1. Preheat: 125 °C - 220 °C, 150 - 210 s at 0.4 k/s to 1.0 k/s
2. Time at T > 220 °C: 60 - 90 s
3. Peak Temperature: 245-250 °C
4. Peak time: 10 - 30 s
5. Cooling rate: ≤ 6 k/s
6. Time from 25 °C to Peak: 240 - 360 s
7. Intel recommends a maximum solder void of 50% after reflow.

**Figure 12-8 Typical Profile Band**

**Note:** Contact your Intel Field Service Representative for any designs unable to meet the recommended guidance for E-pad implementation.



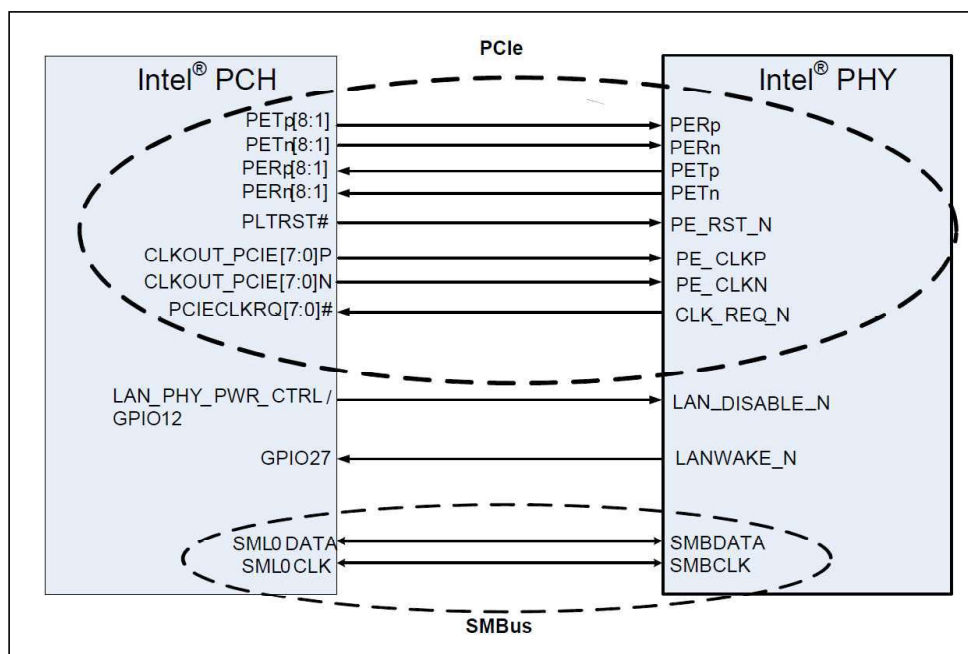
## 12.3 PCH-SMBus/PCIe LOM Design Guidelines

This section contains guidelines on how to implement a PCH/PHY single solution on a system motherboard. It should not be treated as a specification, and the system designer must ensure through simulations or other techniques that the system meets the specified timings. The following are guidelines for both PCH SMBus and PCIe interfaces. Note that PCIe is only applicable to the PHY.

The SMBus/PCIe Interface between the PCH and PHY is shown at high level in [Figure 12-9](#). For complete design details, always refer to the *Intel® Ethernet Connection I219 Reference Schematic*.

**Note:** Board designers MUST select the available PCIe lane based on a specific platform PCH External Design Specification (EDS). Not all PCIe lanes on a PCH are available to connect the I219 GbE PHY to the PCIe interface. For example, The SKL U/Y PCH EDS requires the I219 to only connect to PCIe ports 3, 4, 5, 9, and 10. Contact your local Intel representative for more details.

Refer to [Section 12.6](#) for PCI Express Routing Guidelines.



### Notes:

1. Not all PCH PCIe ports can be used for the I219. Refer to the SkyLake/Greenlow/Purley EDS documentation for the specific ports that can be used with the I219.
2. Any CLKOUT\_PCIE and PCIECLKRQ ports can be used to connect to the I219. These can be selected using the FITC tool.
3. PETp/n, PERp/n, PE\_CLKp/n should be routed as a differential pair as indicated in the PCIe specification.
4. Refer to the I219 reference schematics and design checklists for more details.

**Figure 12-9 Single Solution Interconnect**



## 12.4 SMBus Design Considerations

No single SMBus design solution works for all platforms. Designers must consider the total bus capacitance and device capabilities when designing SMBus segments. Routing SMBus to the PCI slots makes the design process even more challenging since they add so much capacitance to the bus. This extra capacitance has a large affect on the bus time constant which in turn affects the bus rise and fall times.

Primary considerations in the design process are:

- Amount of  $V_{CC\_SUS3\_3}$  current available, that is, minimizing load of  $V_{CC\_SUS3\_3}$ .
- The pull-up resistor size for the SMBus data and clock signals is dependent on the bus load (this includes all device leakage currents). Generally the SMBus device that can sink the least amount of current is the limiting agent on how small the resistor can be. The pull-up resistor cannot be made so large that the bus time constant (Resistance X Capacitance) does not meet the SMBus rise and time specification.
- The maximum bus capacitance that a physical segment can reach is 400 pF.
- SMBus devices that can operate in STR must be powered by the  $V_{CC\_SUS3\_3}$  supply.
- It is recommended that I<sup>2</sup>C (Inter-Integrated Circuit) devices be powered by the  $V_{CC\_core}$  supply. During an SMBus transaction in which the device is sending information to the integrated MAC, the device may not release the SMBus if the integrated MAC receives an asynchronous reset.  $V_{CC\_core}$  is used to enable the BIOS to reset the device if necessary. SMBus 2.0-compliant devices have a timeout capability that makes them in-susceptible to this I<sup>2</sup>C issue, enabling flexibility in choosing a voltage supply.
- No other devices (except the integrated MAC and pull-up resistors) should be connected to the SMBus that connects to the PHY.
- **For system LAN on motherboard (LOM) designs:** The traces should be less than 70 inches for stripline and less than 100 inches for Microstrip. These numbers depend on the stackup, dielectric layer thickness, and trace width. The total capacitance on the trace and input buffers should be under 400 pF.
- **For system LAN on daughterboard designs:** Being conservative, the traces should be less than 7 inches for stripline designs and less than 10 inches for Microstrip designs. The lengths depend on the stackup, dielectric layer thickness, and trace width. Longer traces can be used as long as the total capacitance on the trace and input buffers is under 30 pF.

Note: Refer to [Section 12.1.3](#) for additional SMBus design considerations.

## 12.5 General Layout Guidelines

PHY interface signals must be carefully routed on the motherboard to meet the timing and signal quality requirements of their respective interface specifications. The following are some general guidelines that should be followed in designing a LAN solution. It is recommended that the board designer simulate the board routing to verify that the specifications are met for flight times and skews due to trace mismatch and crosstalk.



## 12.6 Layout Considerations

Critical signal traces should be kept as short as possible to decrease the likelihood of effects by high frequency noise of other signals, including noise carried on power and ground planes. This can also reduce capacitive loading.

Since the transmission line medium extends onto the printed circuit board, layout and routing of differential signal pairs must be done carefully.

Designing for GbE (1000BASE-T) operation is very similar to designing for 10/100 Mb/s. For the PHY, system level tests should be performed at all three speeds.

## 12.7 Guidelines for Component Placement

Component placement can affect signal quality, emissions, and component operating temperature. Careful component placement can:

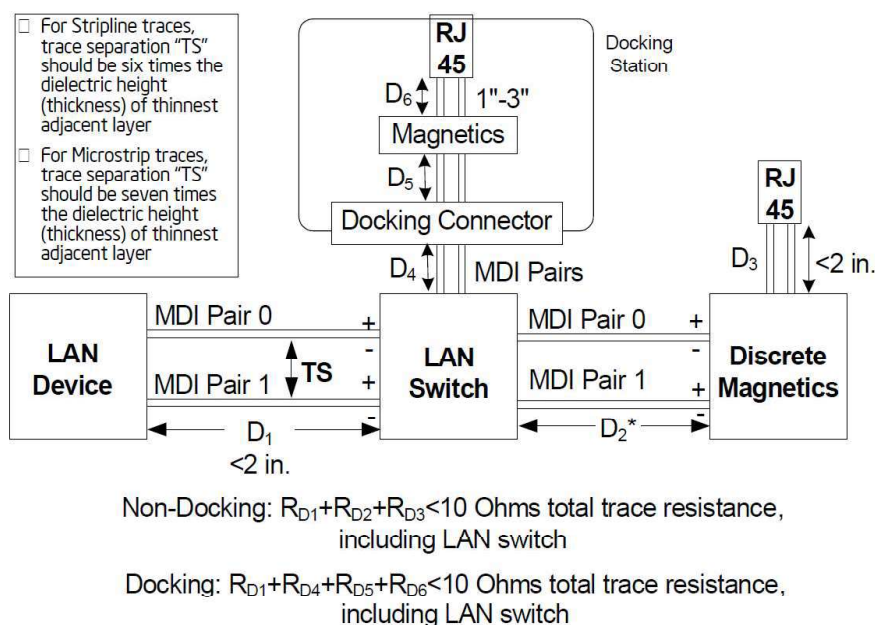
- Decrease potential problems directly related to electromagnetic interference (EMI), which could cause failure to meet applicable government test specifications. In this case, place the PHY more than one inch from the edge of the board.
- Simplify the task of routing traces. To some extent, component orientation affects the complexity of trace routing. The overall objective is to minimize turns and crossovers between traces.

### 12.7.1 PHY Placement Recommendations

Minimizing the amount of space needed for the PHY is important because other interfaces compete for physical space on a motherboard near the connector. The PHY circuits need to be as close as possible to the connector.

[Figure 12-10](#) illustrates some basic placement distance guidelines. To simplify the diagram, it shows only two differential pairs, but the layout can be generalized for a GbE system with four analog pairs. The ideal placement for the PHY (LAN silicon) is approximately one inch behind the magnetics module.

While it is generally a good idea to minimize lengths and distances, [Figure 12-10](#) also illustrates the need to keep the PHY away from the edge of the board and the magnetics module for best EMI performance.



\* This distance is variable and follows the general guidelines.

**Figure 12-10 LAN Device Placement: At Least One Inch from Chassis Openings or Unshielded Connectors—Mobile**

The PHY, referred to as "LAN Device" in Figure 12-10, must be at least one inch from any chassis openings. To help reduce EMI, the following recommendations should be followed:

- Minimize the length of the MDI interface. See detail in Table 12-9 on page 221.
- Place the MDI traces no closer than 0.5 inch (1.3 cm) from the board edge.
- The I219 must be placed greater than 1" away from any hole to the outside of the chassis larger than 0.125 inches (125 mils) The larger the hole the higher the probability the EMI and ESD immunity will be negatively affected.
- The I219 should be placed greater than 250 mils from the board edge.
- If the connector or integrated magnetics module is not shielded, the I219 should be placed at least one inch from the magnetics (if a LAN switch is not used).
- Placing the I219 closer than one inch to unshielded magnetics or connectors increases the probability of failed EMI and common mode noise. If the LAN switch is too far away, it negatively affects IEEE return loss performance.
- The RBIAS trace length must be less than one inch.
- Place the crystal less than one inch (2.54 cm) from the PHY.



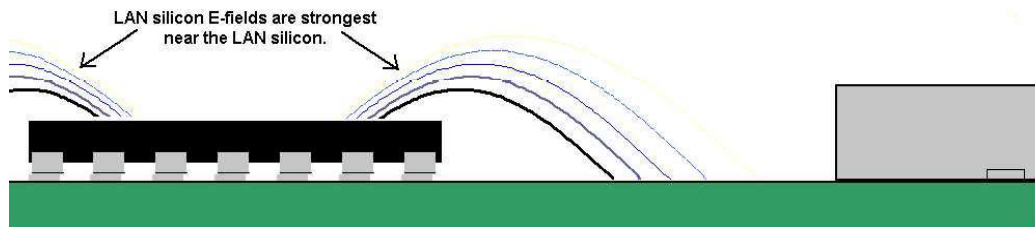


Figure 12-11 PLC Placement: At Least One Inch from I/O Backplane

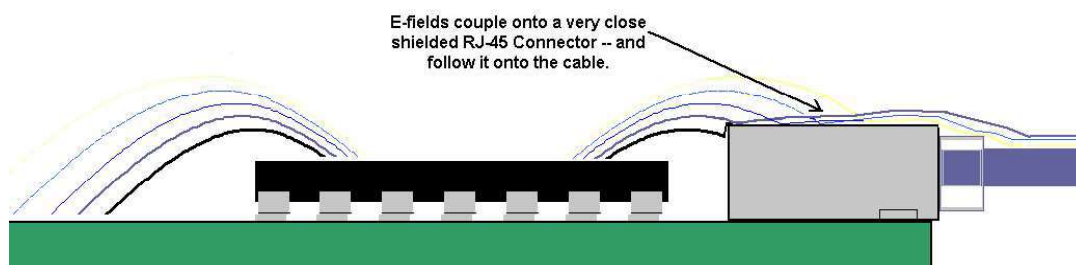


Figure 12-12 Effect of LAN Device Placed Too Close to an RJ-45 Connector or Chassis Opening

## 12.8 MDI Differential-Pair Trace Routing for LAN Design

Trace routing considerations are important to minimize the effects of crosstalk and propagation delays on sections of the board where high-speed signals exist. Signal traces should be kept as short as possible to decrease interference from other signals, including those propagated through power and ground planes.

## 12.9 Signal Trace Geometry

One of the key factors in controlling trace EMI radiation are the trace length and the ratio of trace-width to trace-height above the reference plane. To minimize trace inductance, high-speed signals and signal layers that are close to a reference or power plane should be as short and wide as practical. Ideally, the trace-width to trace-height above the ground plane ratio is between 1:1 and 3:1. To maintain trace impedance, the width of the trace should be modified when changing from one board layer to another if the two layers are not equidistant from the neighboring planes.

Each pair of signals should have a differential impedance of  $100\ \Omega \pm 15\%$ .

A set of trace length calculation tools are available from Intel to aid with MDI topology design. For access to documentation contact your Intel representative.





When performing a board layout, the automatic router feature of the CAD tool must not route the differential pairs without intervention. In most cases, the differential pairs will require manual routing.

**Note:** Measuring trace impedance for layout designs targeting 100  $\Omega$  often results in lower actual impedance due to over-etching. Designers should verify actual trace impedance and adjust the layout accordingly. If the actual impedance is consistently low, a target of 105  $\Omega$  to 110  $\Omega$  should compensate for over-etching.

It is necessary to compensate for trace-to-trace edge coupling, which can lower the differential impedance by up to 10  $\Omega$  when the traces within a pair are closer than 30 mils (edge-to-edge).

**Table 12-9 MDI Routing Summary**

Parameter	Main Route Guidelines	Breakout Guidelines <sup>1</sup>	Notes
Signal group	MDI_PLUS[0:3] MDI_MINUS[0:3]		
Microstrip/stripline uncoupled single-ended impedance specification	50 $\Omega \pm 10\%$		
Microstrip/stripline uncoupled differential impedance specification	100 $\Omega \pm 15\%$		2, 3
Microstrip nominal trace width	Design dependent	Design dependent	4
Microstrip nominal trace space	Design dependent	Design dependent	3, 5
Microstrip/stripline trace length	8 in (203 mm) maximum		6, 7
Microstrip pair-to-pair space (edge-to-edge)	$\geq 7$ times the thickness of the thinnest adjacent dielectric layer		Figure 12-13
Stripline pair-to-pair space (edge-to-edge)	$\geq 6$ times the thickness of the thinnest adjacent dielectric layer		
Microstrip bus-to-bus spacing	$\geq 7$ times the thickness of the thinnest adjacent dielectric layer		
Stripline bus-to-bus spacing	$\geq 6$ times the thickness of the thinnest adjacent dielectric layer		

**Notes:**

1. Pair-to-pair spacing 3 times the dielectric thickness for a maximum distance of 500 mils from the pin.
2. Board designers should ideally target 100  $\Omega \pm 15\%$ . If it's not feasible (due to board stack-up) it is recommended that board designers use a 95  $\Omega \pm 10\%$  target differential impedance for MDI with the expectation that the center of the impedance is always targeted at 95  $\Omega$ . The  $\pm 10\%$  tolerance is provided to allow for board manufacturing process variations and not lower target impedances. The minimum value of impedance cannot be lower than 85  $\Omega$ .
3. Simulation shows 80  $\Omega$  differential trace impedances degrade MDI return loss measurements by approximately 1 dB from that of 90  $\Omega$ .
4. Stripline is NOT recommended due to thinner more resistive signal layers.
5. Use a minimum of 21 mil (0.533 mm) pair-to-pair spacing for board designs that use the CRB design stack-up. Using dielectrics that are thicker than the CRB stack-up might require larger pair-to-pair spacing.
6. For applications that require a longer MDI trace length of more than 8 inches (20.32 mm), it is recommended that thicker dielectric or lower Er materials be used. This permits higher differential trace impedance and wider, lower loss traces. Refer to Table 12-10 for examples of microstrip trace geometries for common circuit board materials.
7. If a LAN switch is not used, the maximum trace length is 4 inches (102 mm). Mobile designs without LAN switch can range up to ~8 inches. Refer to Table 12-10 for trace length information.



**Table 12-10 Maximum Trace Lengths Based on Trace Geometry and Board Stack-Up**

Dielectric Thickness (mils)	Dielectric Constant (DK) at 1 MHz	Width / Space/ Width (mils)	Pair-to-Pair Space (mils)	Nominal Impedance (Ohms)	Impedance Tolerance (±%)	Maximum Trace Length (inches) <sup>1</sup>
2.7	4.05	4/10/4	19	95 <sup>2</sup>	17 <sup>2</sup>	3.5
2.7	4.05	4/10/4	19	95 <sup>2</sup>	15 <sup>2</sup>	4
2.7	4.05	4/10/4	19	95	10	5
3.3	4.1	4.2/9/4.2	23	100 <sup>2</sup>	17 <sup>2</sup>	4
3.3	4.1	4.2/9/4.2	23	100	15	4.6
3.3	4.1	4.2/9/4.2	23	100	10	6
4	4.2	5/9/5	28	100 <sup>2</sup>	17 <sup>2</sup>	4.5
4	4.2	5/9/5	28	100	15	5.3
4	4.2	5/9/5	28	100	10	7

1. Longer MDI trace lengths may be achievable, but may make it more difficult to achieve IEEE conformance. Simulations have shown deviations are possible if traces are kept short. Longer traces are possible; use cost considerations and stack-up tolerance for differential pairs to determine length requirements.
2. Deviations from 100 Ω nominal and/or tolerances greater than 15% decrease the maximum length for IEEE conformance.

**Note:** Use the MDI Differential Trace Calculator to determine the maximum MDI trace length for your trace geometry and board stack-up. Contact your Intel Field Service Representative for access.

The following factors can limit the maximum MDI differential trace lengths for IEEE conformance:

- Dielectric thickness.
- Dielectric constant.
- Nominal differential trace impedance.
- Trace impedance tolerance.
- Copper trace losses.
- Additional devices, such as switches, in the MDI path may impact IEEE conformance.

Board geometry should also be factored in when setting trace length.

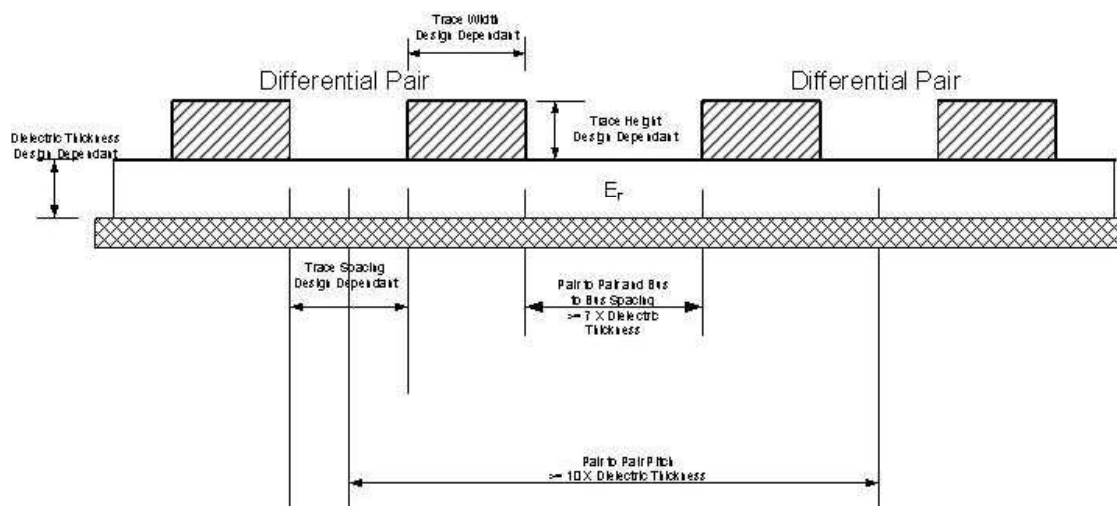


Figure 12-13 MDI Trace Geometry

## 12.10 Trace Length and Symmetry

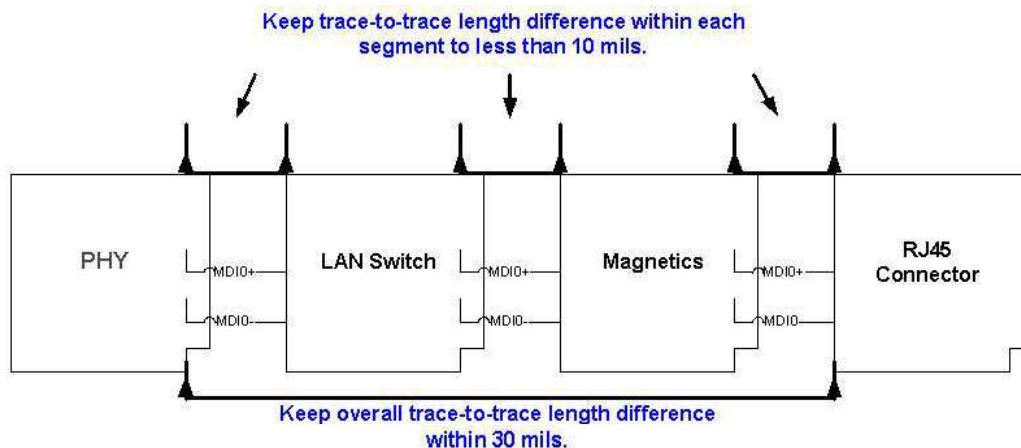
The differential traces should be equal in total length to within 10 mils (0.254 mm) per segment within each pair and as symmetrical as possible. Asymmetrical and unequal length traces in the differential pairs contribute to common mode noise. If a choice has to be made between matching lengths and fixing symmetry, more emphasis should be placed on fixing symmetry. Common mode noise can degrade the receive circuit's performance and contribute to radiated emissions.

The intra-pair length matching on the pairs must be within 10 mils on a segment by segment basis. An MDI segment is defined as any trace within the same layer. For example, transitioning from one layer to another through a via is considered as two separate MDI segments.

The end to end total trace lengths within each differential pair must match as shown in Figure 12-13. The end to end trace length is defined as the total MDI length from one component to another regardless of layer transitions.

The pair to pair length matching is not as critical as the intra-pair length matching but it should be within 2 inches.

When using Microstrip, the MDI traces should be at least 7x the thinnest adjacent dielectric away from the edge of an adjacent reference plane. When using stripline, the MDI traces should be at least 6x the thinnest adjacent dielectric away from the edge of an adjacent reference plane.



**Figure 12-14 MDI Differential Trace Geometry**

**Note:** Similar topology applies to MDI routing from the I219 to the dock RJ45 connector.

## 12.11 Impedance Discontinuities

Impedance discontinuities cause unwanted signal reflections. Vias (signal through holes) and other transmission line irregularities should be minimized. If vias must be used, a reasonable budget is four or less per differential trace. Unused pads and stub traces should also be avoided.

## 12.12 Reducing Circuit Inductance

Traces should be routed over a continuous reference plane with no interruptions. If there are vacant areas on a reference or power plane, the signal conductors should not cross the vacant area. This causes impedance mismatches and associated radiated noise levels.

## 12.13 Signal Isolation

Also, keep the MDI traces away from the edge of an adjacent reference plane by a distance that is at least 7x the thickness of the thinnest adjacent dielectric layer (7x when using Microstrip; 6x when using stripline). If digital signals on other board layers cannot be separated by a ground plane, they should be routed perpendicular to the differential pairs. If there is another LAN controller on the board, the differential pairs from that circuit must be kept away.



Other rules to follow for signal isolation include:

- Separate and group signals by function on separate layers if possible. If possible, maintain at least a gap of 30 mils between all differential pairs (Ethernet) and other nets, but group associated differential pairs together.
- Physically group together all components associated with one clock trace to reduce trace length and radiation.
- Isolate I/O signals from high-speed signals to minimize crosstalk, which can increase EMI emission and susceptibility to EMI from other signals.
- Avoid routing high-speed LAN traces near other high-frequency signals associated with a video controller, cache controller, processor, switching power supplies, or other similar devices.

## 12.14 Power and Ground Planes

Good grounding requires minimizing inductance levels in the interconnections and keeping ground returns short, signal loop areas small, and power inputs bypassed to signal return. This will significantly reduce EMI radiation.

The following guidelines help reduce circuit inductance in both backplanes and motherboards:

- Route traces over a continuous plane with no interruptions. Do not route over a split power or ground plane. If there are vacant areas on a ground or power plane, avoid routing signals over the vacant area. This will increase inductance and EMI radiation levels.
- All ground vias should be connected to every ground plane; and every power via, to all power planes at equal potential. This helps reduce circuit inductance.
- Physically locate grounds between a signal path and its return. This will minimize the loop area.
- Split the ground plane beneath a magnetics module. The RJ-45 connector side of the transformer module should have chassis ground beneath it.

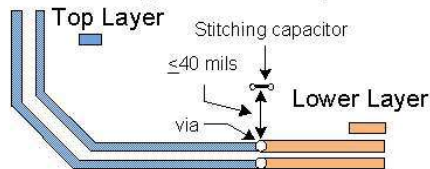
**Caution:** DO NOT do this if the RJ-45 connector has integrated USB.

**Note:** All impedance-controlled signals should be routed in reference to a solid plane. If there are plane splits on a reference layer and the signal traces cross those splits, stitching capacitors should be used within 40 mils of where the crossing occurs. See [Figure 12-15](#).

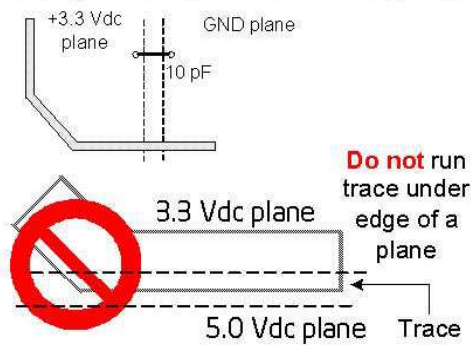
If signals transition from one reference layer to another reference layer then stitching capacitors or connecting vias should be used based on the following:

- If the transition is from power-referenced layer to a ground-referenced layer or from one voltage-power referenced layer to a different voltage-power referenced layer, then stitching capacitors should be used within 40 mils of the transition.
- If the transition is from one ground-referenced layer to another ground-referenced layer or is from a power-referenced layer to the same net power-referenced layer, then connecting vias should be used within 40 mils of the transition.

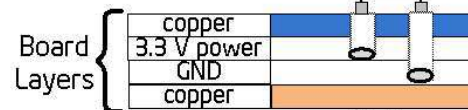
### Transitioning Reference Layers



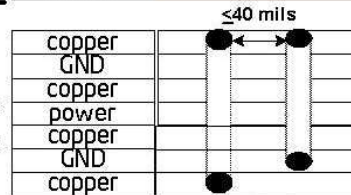
### Crossing Plane Splits-Use Stitching Capacitors



Distance from stitching capacitor to any via is  $\leq 40$  mils



Connection Vias  
GND to GND



Connection Vias  
PWR to same PWR

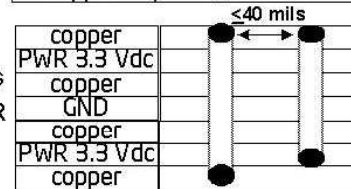


Figure 12-15 Trace Transitioning Layers and Crossing Plane Splits

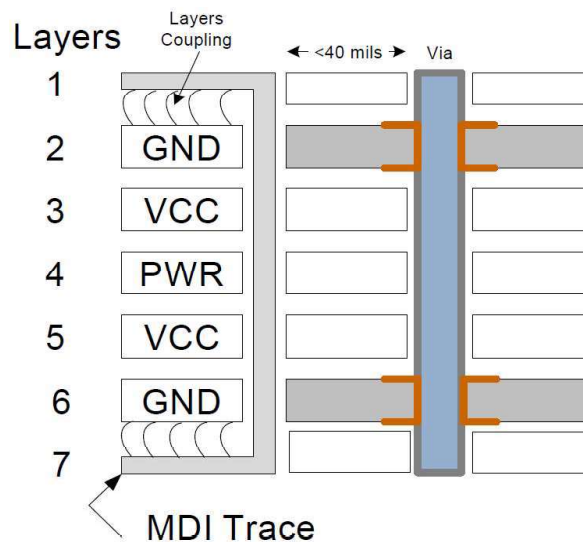


Figure 12-16 Via Connecting GND to GND

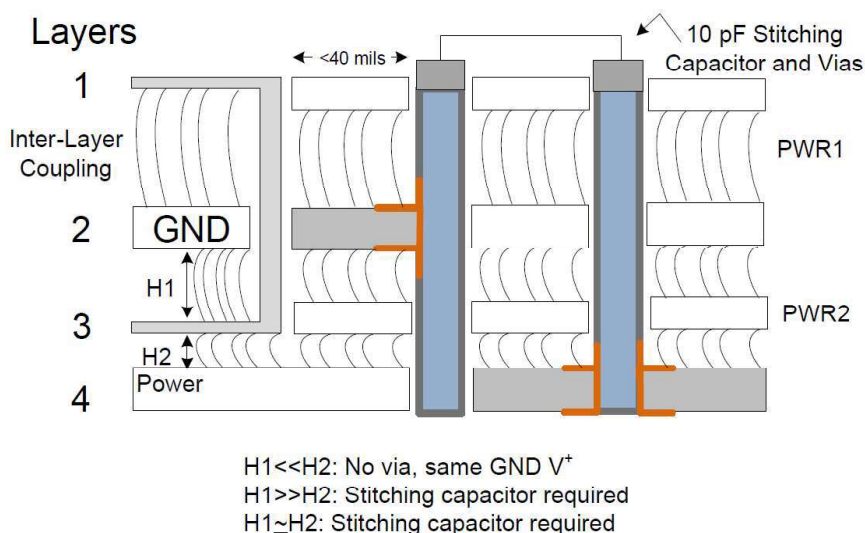


Figure 12-17 Stitching Capacitor Between Vias Connecting GND to GND

## 12.15 Traces for Decoupling Capacitors

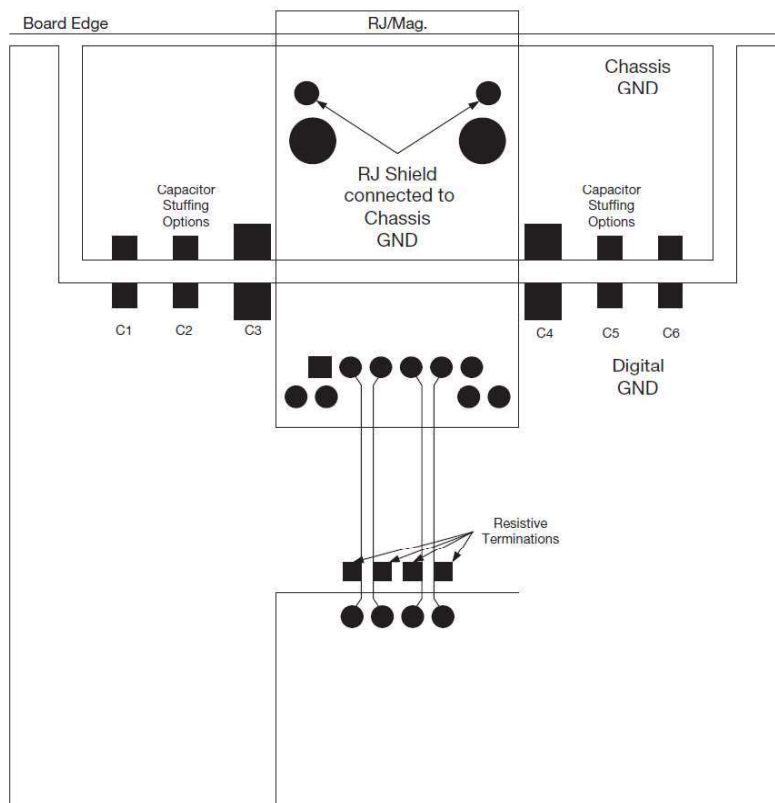
Traces between decoupling and I/O filter capacitors should be as short and wide as practical. Long and thin traces are more inductive and reduce the intended effect of decoupling capacitors. Also, for similar reasons, traces to I/O signals and signal terminations should be as short as possible. Vias to the decoupling capacitors should be sufficiently large in diameter to decrease series inductance. Refer to the Power Delivery section for the PHY in regards to actual placement requirements of the capacitors.

## 12.16 Ground Planes Under a Magnetics Module

The magnetics module chassis or output ground (secondary side of transformer) should be separated from the digital or input ground (primary side) by a physical separation of 100 mils minimum. Splitting the ground planes beneath the transformer minimizes noise coupling between the primary and secondary sides of the transformer and between the adjacent coils in the magnetics. This arrangement also improves the common mode choke functionality of magnetics module.

**Caution:** DO NOT do this if the RJ-45 connector has integrated USB.

Figure 12-18 shows the preferred method for implementing a ground split under an integrated magnetics module/RJ-45 connector.



**Figure 12-18** Ideal Ground Split Implementation

**Table 12-11** Capacitor Stuffing Option Recommended Values

Capacitors	Value
C3, C4	4.7 $\mu$ F or 10 $\mu$ F
C1, C2, C5, C6	470 pF to 0.1 $\mu$ F

The placement of C1 through C6 may also differ for each board design (in other words, not all of the capacitors may need to be populated). Also, the capacitors may not be needed on both sides of the magnetics module.

**Note:** If using an integrated magnetics module without USB, provide a separate chassis ground "island" to ground around the RJ-45 connector. The split in the ground plane should be at least 20 mils wide.

Some integrated magnetics modules/RJ-45 connectors have recently incorporated the USB into the device. For this type of magnetics module, a chassis ground moat may not be feasible due to the digital ground required for the USB pins and their placement relative to the magnetics pins. Thus, a continuous digital ground without any moats or splits must be used. [Figure 12-19](#) provides an example of this.



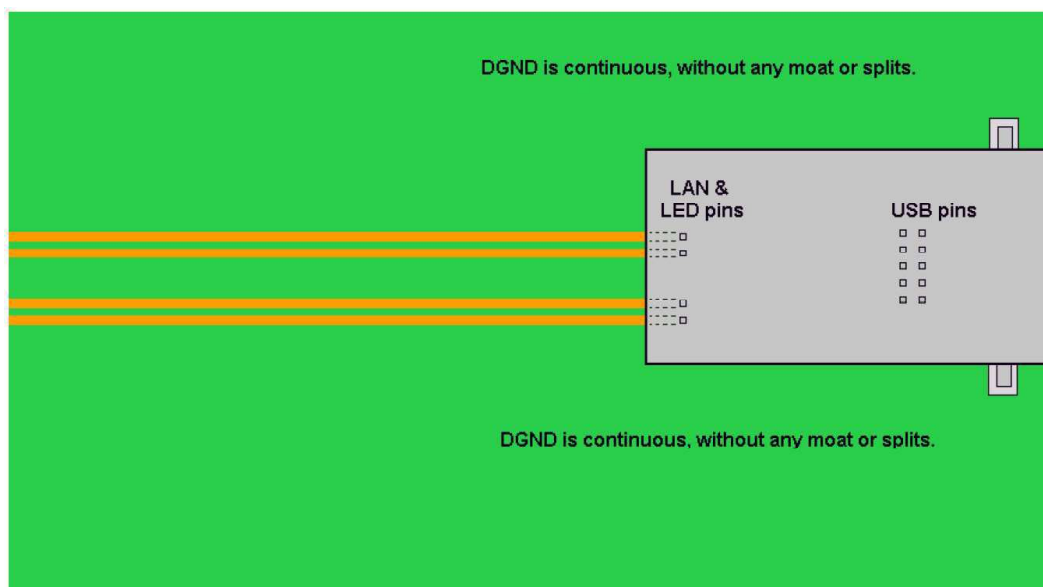


Figure 12-19 Ground Layout with USB

## 12.17 Light Emitting Diodes

The device has three high-current outputs to directly drive LEDs for link, activity and speed indication. Since LEDs are likely to be integral to a magnetics module, take care to route the LED traces away from potential sources of EMI noise. In some cases, it may be desirable to attach filter capacitors.

LAN LED traces should be placed at least 6x (side by side separation) the dielectric height from sources of noise (ex: signaling traces) and susceptible signal traces (ex: reset signals) on the same or adjacent layers.

LAN LED traces should be placed at least 7x (broadside coupling) the dielectric height from sources of noise (ex: signaling traces) and susceptible signal traces (ex: reset signals) on the same or adjacent layers.

## 12.18 Considerations for Layout

The PHY MDI routing using microstrip requires a differential impedance of  $100\ \Omega \pm 15\%$ . A 35-mil (0.889 mm) separation is required between pairs. The 35-mil separation can be reduced for 24 mils (0.61 mm) in breakout routing. All MDI traces must be referenced to ground.



## 12.19 Frequency Control Device Design Considerations

This section provides information regarding frequency control devices, including crystals and oscillators, for use with all Intel Ethernet controllers. Several suitable frequency control devices are available; none of which present any unusual challenges in selection. The concepts documented within this section are applicable to other data communication circuits, including the PHY.

The PHY contains amplifiers that form the basis for feedback oscillators when they are used with the specific external components. These oscillator circuits, which are both economical and reliable, are described in more detail in [Section 12.20.3](#).

The chosen frequency control device vendor should be consulted early in the design cycle. Crystal and oscillator manufacturers familiar with networking equipment clock requirements may provide assistance in selecting an optimum, low-cost solution.

Several types of third-party frequency reference components are currently available. Descriptions of each type follow in subsequent sections. They are also listed in order of preference.

## 12.20 Crystals and Oscillators

Clock sources should not be placed near I/O ports or board edges. Radiation from these devices may be coupled onto the I/O ports or out of the system chassis. Crystals should also be kept away from the Ethernet magnetics module to prevent interference.

Crystal and load capacitors should be placed on the printed circuit boards as close to the PHY as possible, which is within 1.0 inch. Traces from XTAL\_IN (X1) and XTAL\_OUT (X2) should be routed as symmetrically as possible. Do not route X1 and X2 as a differential trace. Doing so increases jitter and degrades LAN performance.

- The crystal trace lengths should be less than 1 inch.
- The crystal load capacitors should be placed less than 1" from the crystal.
- The clock lines must be at least 5 times the height of the thinnest adjacent dielectric layer away from other digital traces (especially reset signals), I/O ports, board edge, transformers and differential pairs.
- The clock lines must not cross any plane cuts on adjacent power or ground reference layers unless there are decoupling capacitors or connecting vias near the transition.
- The clock lines should not cross or run in parallel (within 3x the dielectric thickness of the closest dielectric layer) with any trace (100 MHz signal or higher) on an adjacent layer.

### 12.20.1 Quartz Crystal

Quartz crystals are generally considered to be the mainstay of frequency control components due to their low cost and ease of implementation. They are available from numerous vendors in many package types and with various specification options.



## 12.20.2 Fixed Crystal Oscillator

A packaged fixed crystal oscillator comprises of an inverter, a quartz crystal, and passive components conveniently packaged together. The device renders a strong, consistent square wave output. Oscillators used with microprocessors are supplied in many configurations and tolerances.

Crystal oscillators should be restricted for use in special situations, such as shared clocking among devices or multiple controllers. Since clock routing can be difficult to accomplish, it is preferable to provide a separate crystal for each device.

**Note:** Contact your Intel Field Service Representative to obtain the most current device documentation prior to implementing this solution.

## 12.20.3 Crystal Selection Parameters

All crystals used with Intel Ethernet controllers are described as “AT-cut,” which refers to the angle at which the unit is sliced with respect to the long axis of the quartz stone.

Table 12-12 lists crystals which have been used successfully in past designs. (No particular product is recommended.)

**Table 12-12 Crystal Manufacturers and Part Numbers**

Manufacturer	Part Number	Notes
Epson*	Q22FA1280021400	2.0 x 1.6 x 0.5mm Small part. Loading capacitors = 10 pF.
TXC Corporation, USA*	8Y25000010	2.0 x 1.6 x 0.5mm Small part. Loading capacitors = 10 pF.
TXC Corporation, USA	7M25020011	3.2 x 2.5 x 0.7 mm
TXC Corporation, USA	9C25000008	HC-49S type, SMD (low profile 3 mm)
NDK America, Inc.*	EXS00A-CH00387	3.2 x 2.5 x 0.8 mm
NDK America, Inc.	41CD25.0F1303018	HC-49S type, SMD

The datasheet for the PHY lists the crystal electrical parameters and provides suggested values for typical designs. Designers should refer to criteria outlined in their respective PHY datasheet. The parameters are described in the following subsections.

## 12.20.4 Vibrational Mode

Crystals in the frequency range referenced above are available in both fundamental and third overtone. Unless there is a special need for third overtone, fundamental mode crystals should be used.



## 12.20.5 Nominal Frequency

Intel Ethernet controllers use a crystal frequency of 25.000 MHz. The 25 MHz input is used to generate a 125-MHz transmit clock for 100BASE-TX and 1000BASE-TX operation, and 10-MHz and 20-MHz transmit clocks, for 10BASE-T operation.

## 12.20.6 Frequency Tolerance

The frequency tolerance for an Ethernet Platform LAN Connect device is dictated by the IEEE 802.3 specification as  $\pm 50$  parts per million (ppm). This measurement is referenced to a standard temperature of 25 °C. Intel recommends a frequency tolerance of  $\pm 30$  ppm to ensure for any frequency variance contributed by the PCB.

## 12.20.7 Temperature Stability and Environmental Requirements

Temperature stability is a standard measure of how the oscillation frequency varies over the full operational temperature range (and beyond). Several optional temperature ranges are currently available, including -40 °C to +85 °C for industrial environments. Some vendors separate operating temperatures from temperature stability. Manufacturers may also list temperature stability as 50 ppm in their data sheets.

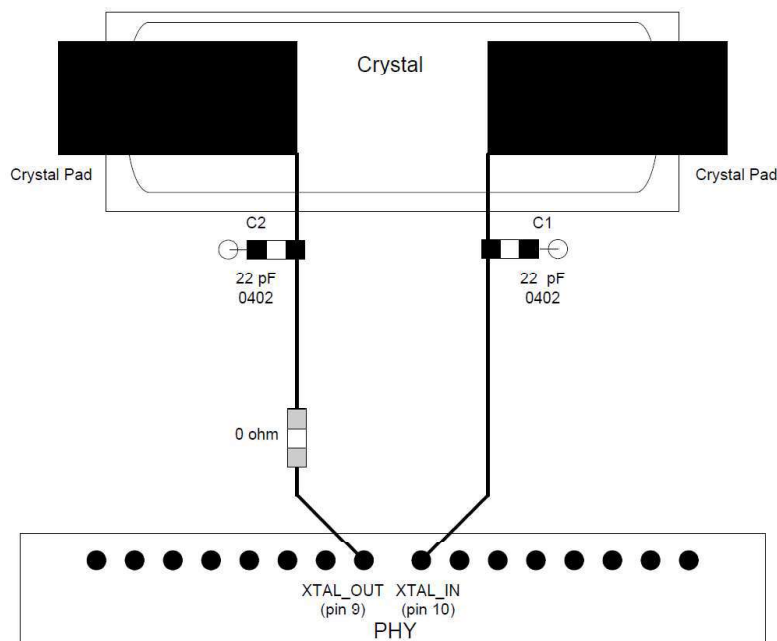
**Note:** Crystals also carry other specifications for storage temperature, shock resistance, and reflow solder conditions. Crystal vendors should be consulted early in the design cycle to discuss its application and environmental requirements.

## 12.20.8 Calibration Mode

The terms “series-resonant” and “parallel-resonant” are often used to describe crystal oscillator circuits. Specifying parallel mode is critical to determining how the crystal frequency is calibrated at the factory.

A crystal specified and tested as series resonant oscillates without problem in a parallel-resonant circuit, but the frequency is higher than nominal by several hundred parts per million. The purpose of adding load capacitors to a crystal oscillator circuit is to establish resonance at a frequency higher than the crystal’s inherent series resonant frequency.

Figure 12-20 illustrates a simplified schematic of the internal oscillator circuit. Pin X1 and X2 refers to XTAL\_IN and XTAL\_OUT in the Ethernet device, respectively. The crystal and the capacitors form a feedback element for the internal inverting amplifier. This combination is called parallel-resonant, because it has positive reactance at the selected frequency. In other words, the crystal behaves like an inductor in a parallel LC circuit. Oscillators with piezoelectric feedback elements are also known as “Pierce” oscillators.



**Figure 12-20 Thermal Oscillator Circuit**

## 12.20.9 Load Capacitance

The formula for crystal load capacitance is as follows:

$$C_L = \frac{(C1 \cdot C2)}{(C1 + C2)} + C_{\text{stray}}$$

where  $C1 = C2 = 22 \text{ pF}$  (as suggested in most Intel reference designs), and  $C_{\text{stray}}$  = allowance for additional capacitance in pads, traces and the chip carrier within the Ethernet device package and  $C_{\text{damp}}$ .

## 12.20.10 Shunt Capacitance

The shunt capacitance parameter is relatively unimportant compared to load capacitance. Shunt capacitance represents the effect of the crystal's mechanical holder and contacts. The shunt capacitance should be a maximum of 6 pF.



## 12.20.11 Equivalent Series Resistance

Equivalent Series Resistance (ESR) is the real component of the crystal's impedance at the calibration frequency, which the inverting amplifier's loop gain must overcome. ESR varies inversely with frequency for a given crystal family. The lower the ESR, the faster the crystal starts up. Crystals with an ESR value of 50  $\Omega$  or better should be used.

## 12.20.12 Drive Level

Drive level refers to power dissipation in use. The allowable drive level for a Surface Mounted Technology (SMT) crystal is less than its through-hole counterpart. This is due to the fact that surface mount crystals are typically made from narrow, rectangular AT strips, rather than circular AT quartz blanks.

When selecting a crystal, board designers must ensure that the crystal specification meets at least the drive level specified. For example, if the crystal drive level specification states that the drive level is 200  $\mu\text{W}$  maximum, then the crystal drive level must be at least 200  $\mu\text{W}$ . So, a 500  $\mu\text{W}$  crystal is sufficient, but a 100  $\mu\text{W}$  crystal is not.

## 12.20.13 Aging

Aging is a permanent change in frequency (and resistance) occurring over time. This parameter is most important in its first year because new crystals age faster than old crystals. Crystals with a maximum value of  $\pm 5$  ppm per year aging should be used.

## 12.20.14 Reference Crystal

The normal tolerances of the discrete crystal components can contribute to small frequency offsets with respect to the target center frequency. To minimize the risk of tolerance-caused frequency offsets causing a small percentage of production line units to be outside of the acceptable frequency range, it is important to account for those shifts while empirically determining the proper values for the discrete loading capacitors, C1 and C2.

Even with a perfect support circuit, most crystals will oscillate slightly higher or lower than the exact center of the target frequency. Therefore, frequency measurements, which determine the correct value for C1 and C2, should be performed with an ideal reference crystal. When the capacitive load is exactly equal to the crystal's load rating, an ideal reference crystal will be perfectly centered at the desired target frequency.



## 12.20.14.1 Reference Crystal Selection

There are several methods available for choosing the appropriate reference crystal:

- If a Saunders and Associates (S&A) crystal network analyzer is available, then discrete crystal components can be tested until one is found with zero or nearly zero ppm deviation (with the appropriate capacitive load). A crystal with zero or near zero ppm deviation will be a good reference crystal to use in subsequent frequency tests to determine the best values for C1 and C2.
- If a crystal analyzer is not available, then the selection of a reference crystal can be done by measuring a statistically valid sample population of crystals, which has units from multiple lots and approved vendors. The crystal, which has an oscillation frequency closest to the center of the distribution, should be the reference crystal used during testing to determine the best values for C1 and C2.
- It may also be possible to ask the approved crystal vendors or manufacturers to provide a reference crystal with zero or nearly zero deviation from the specified frequency when it has the specified  $C_{Load}$  capacitance.

When choosing a crystal, customers must keep in mind that to comply with IEEE specifications for 10/100 Mb/s operation and 10/100/1000 Mb/s operation if applicable, the transmitter reference frequency must be precise within  $\pm 50$  ppm. Intel recommends customers use a transmitter reference frequency that is accurate to within  $\pm 30$  ppm to account for variations in crystal accuracy due to crystal manufacturing tolerance.

## 12.20.14.2 Circuit Board

Since the dielectric layers of the circuit board are allowed some reasonable variation in thickness, the stray capacitance from the printed board (to the crystal circuit) will also vary. If the thickness tolerance for the outer layers of dielectric are controlled within  $\pm 15\%$  of nominal, then the circuit board should not cause more than  $\pm 2$  pF variation to the stray capacitance at the crystal. When tuning crystal frequency, it is recommended that at least three circuit boards are tested for frequency. These boards should be from different production lots of bare circuit boards.

Alternatively, a larger sample population of circuit boards can be used. A larger population will increase the probability of obtaining the full range of possible variations in dielectric thickness and the full range of variation in stray capacitance.

Next, the exact same crystal and discrete load capacitors (C1 and C2) must be soldered onto each board, and the LAN reference frequency should be measured on each circuit board.

The circuit board, which has a LAN reference frequency closest to the center of the frequency distribution, should be used while performing the frequency measurements to select the appropriate value for C1 and C2.

## 12.20.14.3 Temperature Changes

Temperature changes can cause the crystal frequency to shift. Therefore, frequency measurements should be done in the final system chassis across the system's rated operating temperature range.



## 12.20.15 Oscillator Support

The PHY clock input circuit is optimized for use with an external crystal. However, an oscillator can also be used in place of the crystal with the proper design considerations (refer to the PHY Datasheet for detailed clock oscillator specifications):

- The clock oscillator has an internal voltage regulator to isolate it from the external noise of other circuits to minimize jitter. If an external clock is used, this imposes a maximum input clock amplitude. For example, if a 3.3 V DC oscillator is used, its output signal should be attenuated to a maximum value with a resistive divider circuit.
- The input capacitance introduced by the PHY (approximately 11 to 13 pF) is greater than the capacitance specified by a typical oscillator (approximately 15 pF).
- The input clock jitter from the oscillator can impact the PHY clock and its performance.

**Note:** The power consumption of additional circuitry equals about 1.5 mW.

Table 12-13 lists oscillators that can be used with the PHY. Note that no particular oscillator is recommended.

**Table 12-13 Oscillator Manufacturers and Part Numbers**

Manufacturer	Part Number	Notes
TXC Corporation - USA	8W25080004	2,5 x 2,0 x 0,8mm.
TXC Corporation - USA	7X25080001	3,2 x 2,5 x 1,0 mm.

## 12.20.16 Oscillator Placement and Layout Recommendations

Oscillator clock sources should not be placed near I/O ports or board edges. Radiation from these devices can be coupled into the I/O ports and radiate beyond the system chassis. Oscillators should also be kept away from the Ethernet magnetics module to prevent interference.

The oscillator must have its own decoupling capacitors and they must be placed within 0.25 inches. If a power trace is used (not power plane), the trace from the capacitor to the oscillator must not exceed 0.25 inches in length. The decoupling capacitors help to improve the oscillator stability. The oscillator clock trace should be less than two inches from the PHY. If it is greater than 2 inches, then verify the signal quality, jitter, and clock frequency measurements at the PHY.

The clock lines should also target  $5\ \Omega \pm 15\%$  and should have  $10\ \Omega$  series back termination placed close to the series oscillator. To help reduce EMI, the clock lines must be a distance of at least five times the height of the thinnest adjacent dielectric layer away from other digital traces (especially reset signals), I/O ports, the board edge, transformers and differential pairs.

The clock lines must not cross any plane cuts on adjacent power or ground reference layers unless there are decoupling capacitors or connecting vias near the transition. The clock lines should not cross or run in parallel with any trace (100 MHz signal or higher) on an adjacent layer.





There should be a ferrite bead within 250 mils of the oscillator power pin and there must be a 1  $\mu$ F or greater capacitor within 250 mils of the oscillator, connected to the power trace between the oscillator input and ferrite bead. With a ferrite bead on the power trace for the oscillator, there should be a power pour (or fat trace) to supply power to the oscillator.

**Note:** For the latest PHY schematic connection recommendations, refer to the *Intel® Ethernet Connection I219 Reference Schematic* and the *Intel® Ethernet Connection I219 Schematic and Layout Checklist*, available through your Intel representative.

## 12.21 LAN Switch

Table 12-14 lists LAN switches that can be used with the I219. Note that no particular LAN switch is recommended.

**Table 12-14 LAN Switch Manufacturers and Part Numbers**

Manufacturer	Part Number	Notes
Pericom*	PI3L720	7.0 x 3.5 x 0.75 mm. Enhanced ESD.
Pericom	PI3L500-AZ	11.0 x 5.0 x 0.75 mm. Enhanced ESD.
Texas Instruments*	TS3L500AE	11.0 x 5.0 x 0.75 mm. Enhanced ESD.

## 12.22 Troubleshooting Common Physical Layout Issues

The following lists common physical layer design and layout mistakes in LAN on Motherboard (LOM) designs.

1. Lack of symmetry between the two traces within a differential pair. Asymmetry can create common-mode noise and distort the waveforms. For each component and via that one trace encounters, the other trace should encounter the same component or a via at the same distance from the Ethernet silicon.
2. Unequal length of the two traces within a differential pair. Inequalities create common-mode noise and will distort the transmit or receive waveforms.
3. Excessive distance between the Ethernet silicon and the magnetics. Long traces on FR4 fiberglass epoxy substrate will attenuate the analog signals. In addition, any impedance mismatch in the traces will be aggravated if they are longer than the four-inch guideline.
4. Routing any other trace parallel to and close to one of the differential traces. Crosstalk getting onto the receive channel will cause degraded long cable BER. Crosstalk getting onto the transmit channel can cause excessive EMI emissions and can cause poor transmit BER on long cables. At a minimum, for stripline other signals should be kept at least 6x the height of the thinnest adjacent dielectric layer. For microstrip it is 7x. The only possible exceptions are in the vicinities where the traces enter or exit the magnetics, the RJ-45 connector, and the Ethernet silicon.
5. Using a low-quality magnetics module.



6. Reusing an out-of-date physical layer schematic in a Ethernet silicon design. The terminations and decoupling can be different from one PHY to another.
7. Incorrect differential trace impedances. It is important to have about a 100- $\Omega$  impedance between the two traces within a differential pair. This becomes even more important as the differential traces become longer. To calculate differential impedance, many impedance calculators only multiply the single-ended impedance by two. This does not take into account edge-to-edge capacitive coupling between the two traces. When the two traces within a differential pair are kept close to each other, the edge coupling can lower the effective differential impedance by 5  $\Omega$  to 20  $\Omega$ . Short traces will have fewer problems if the differential impedance is slightly off target.

## 12.23 Power Delivery

The I219 requires a 3.3 V power rail and a 0.93 V (Core) power rail. The internal 3.3 V power rail is brought out for decoupling. [Figure 2-2](#) shows a typical power delivery configuration that can be implemented. However, power delivery can be customized based on a specific OEM. In general planes should be used to deliver 3.3 Vdc and the Core voltage. Not using planes can cause resistive voltage drop and/or inductive voltage drop (due to transient or static currents). Some of the symptoms of these voltage drops can include higher EMI, radiated immunity, radiated emissions, IEEE conformance issues, and register corruption.

Decoupling capacitors (0.1  $\mu$ F and smaller) should be placed within 250 mils of the LAN device. They also should be distributed around the PHY and some should be in close proximity to the power pins.

The bulk capacitors (1.0  $\mu$ F or greater) should be placed within 1 inch if using a trace (50 mils wide or wider) or within 1.5 inches if using a plane.

The Core power rail for the I219 uses the integrated SVR (iSVR). When laying out the circuit the inductor must be placed within 0.5" of the input pin to the PHY and connected with a trace wider than or equal to 20 mil wide.

See the reference schematic for further details regarding the Core power rail.

While Intel does not endorse vendors or specific components, design compatibility has been verified for the connectors in [Table 12-15](#).

**Table 12-15 Inductors and Manufacturers**

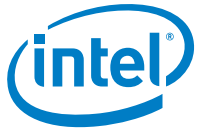
Manufacturer	Part Number	Notes
Taiyo Yuden*	NRS2012T-4R7MGJ	2.0 x 2.0 x 1.2 mm
TDK*	VLS2012ET-4R7M	2.0 x 2.0 x 1.2 mm
muRata*	LQH32PN4R7NN0	3.2 x 2.5 x 1.55 mm
muRata	LQH32CN4R7M53	3.2 x 2.5 x 1.55 mm

**Note:** For latest PHY schematic connection recommendations, refer to the *Intel® I219 GbE PHY Reference Schematic* or contact your Intel Field Service Representative.



## **12.24 I219 Power Sequencing**

The Intel® Ethernet Controller I219 does not require any power sequencing between the 3.3 V and Core power rails. See the reference schematic for details.



**NOTE:**      *This page intentionally left blank.*



## 13.0 Non-Mobile Design Considerations and Guidelines

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The PCH incorporates an integrated 10/100/1000 Mb/s MAC controller that can be used with an external Intel® Ethernet Connection I219 (PHY) shown in [Figure 13-1](#). Its bus master capabilities enable the component to process high-level commands and perform multiple operations, which lowers processor use by offloading communication tasks from the processor.

The PCH, which hereinafter refers to the integrated MAC within the PCH, supports the SMBus interface for manageability while in an Sx state and PCI Express\* (PCIe\*) for 10/100/1000 Mb/s traffic in an S0 state.

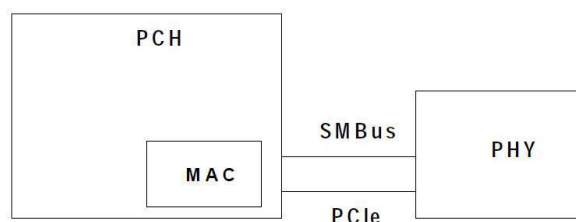
**Note:** The PCIe interface is not PCIe-compliant. It operates at half of the PCI Express\* (PCIe\*) Specification v1.0 (2.5 GT/s) speed. In this section, the term “PCIe-based” is interchangeable with “PCIe.” There are no design layout differences between normal PCIe and the PCIe-based interface.

The PHY interfaces with the integrated MAC through two interfaces: PCIe and SMBus. In SMBus mode, the link speed is reduced to 10 Mb/s. The PCIe interface incorporates two aspects: a PCIe-based SerDes (electrically) and a custom logic protocol for messaging between the integrated MAC and the PHY.

**Note:** Gigabit Ethernet requires an SPI Flash to host firmware and does not work without an SPI Flash on board.

The integrated MAC supports multi-speed operation (10/100/1000 Mb/s). The integrated MAC also operates in full-duplex at all supported speeds or half-duplex at 10/100 Mb/s as well as adhering to the IEEE 802.3x Flow Control Specification.

**Note:** References to the AUX power rail means the power rail is available in all power states including G3 to S5 transitions and Sx states with Wake on LAN (WoL) enabled. For example, V3P3\_AUX in this section refers to a rail that is powered under the conditions previously mentioned.



**Figure 13-1 PCH/PHY Interface Connections**



**Table 13-1 SMBus Data Signals on the PCH**

Group	PHY Signal Name	PCH Signal Name	Description
Data	SMB_DATA	SMLINK0_DATA	SMBus data

**Table 13-2 PCIe Data Signals on the PCH**

Group	PHY Signal Name	PCH Signal Name	Description
Data	PETp PETn	PETp PETn	PCIe transmit pair
Data	PERp PERn	PERp PERn	PCIe receive pair

**Note:** The appropriate NVM descriptor soft strap (PCHSTRP9) should define which PCIe port is configured as GbE LAN. Refer to the PCH EDS document for the specific ports that can be used for GbE LAN.

**Table 13-3 PCIe Data Signals on the PCH**

Group	PHY Signal Name	PCH Signal Name	Description
Clock	SMB_CLK	SML0_CLK	SMBus clock.
Clock	PE_CLKP PE_CLKN	CLKOUT_PCIE[7:0]_P <sup>1</sup> CLKOUT_PCIE[7:0]_N <sup>1</sup>	PCIe clock.
Clock	CLK_REQ_N	PCIECLKRQ[7:0]#	PCIe clock request.
Reset	PE_RST_N	PLTRST#	PCIe reset.

1. These signals come from the PCH and drive the PHY.

## 13.1 PHY Overview

The PHY is a single port compact component designed for 10/100/1000 Mb/s operation. It enables a single port Gigabit Ethernet (GbE) implementation in a very small area, easing routing constraints from the PCH chipset to the PHY.

The PHY provides a standard IEEE 802.3 Ethernet interface for 1000BASE-T, 100BASETX, and 10BASE-T applications (802.3ab, 802.3u, and 802.3i, respectively).

### 13.1.1 PHY Interconnects

The main interfaces for either PHY are PCIe and SMBus on the host side and Media Dependent Interface (MDI) on the link side. Transmit traffic is received from the PCH as either PCIe or SMBus packets on the host interconnect and transmitted as Ethernet packets on the MDI link. Receive traffic arrives as Ethernet packets on the MDI link and transferred to the PCH through either the PCIe or SMBus interconnects.

The PHY switches the in-band traffic automatically between PCIe and SMBus based on platform reset. The transition protocol is done through SMBus. The PCIe interface is powered down when the Ethernet link is running in an Sx state.



## 13.1.2 PCIe-Based Interface

A high-speed SerDes interface uses PCIe electrical signaling at half speed while utilizing a custom logical protocol for active state operation mode.

**Note:** PCIe validation tools cannot be used for electrical validation of this interface. However, PCIe layout rules apply for on-board routing.

### 13.1.2.1 PCIe Interface Signals

The signals used to connect between the PCH and the PHY in this mode are:

- Serial differential pair running at 1.25 Gb/s for Rx.
- Serial differential pair running at 1.25 Gb/s for Tx.
- 100-MHz differential clock input to the PHY is generated by the PCH.
- Power and clock good indication to the PHY PE\_RST\_N.
- Clock control through CLK\_REQ\_N (see [Table 13-3](#)). This PHY output should be tied to the PCH input and pulled up with a 10 K $\Omega$  resistor connected to 3.3 V DC AUX power (present in G3 to S5).

### 13.1.2.2 PCIe Operation and Channel Behavior

The PHY runs only at 1250 Mb/s speed; 1/2 the Gen 1, 2.5 Gb/s PCIe frequency. Each PCIe root port in the PCH has the ability to run at 1250 Mb/s. The configuration for a PCH PCIe port attached to a PCIe Intel PHY device is pre-loaded from the GbE region of the NVM. The selected port adjusts the transmitter to run at 1/2 the Gen 1 PCIe speed and does not need to be PCIe compliant.

Packets transmitted and received over the PCIe interface are full Ethernet packets and not PCIe transaction/link/physical layer packets.

### 13.1.2.3 PCIe Connectivity

The PHY transmit/receive pins are output/input signals and are connected to the PCH as listed in [Table 13-1](#) through [Table 13-3](#).

### 13.1.2.4 PCIe Reference Clock

The PCIe Interface uses a 100-MHz differential reference clock, denoted PE\_CLKP and PE\_CLKN. This signal is typically generated on the platform and routed to the PCIe port.

The frequency tolerance for the PCIe reference clock is  $\pm 300$  ppm.



### 13.1.3 SMBus Interface

SMBus is a low speed (100/400/1000 KHz) serial bus used to connect various components in a system. SMBus is used as an interface to pass traffic between the PHY and the PCH when the platform is in a low power state (Sx). The interface is also used to enable the PCH to configure the PHY as well as pass in-band information between them.

The SMBus uses two primary signals to communicate: SMBCLK and SMBDATA. Both of these signals float high with board-level  $499\ \Omega \pm 5\%$  pull-up resistors.

#### 13.1.3.1 SMBus Connectivity

Table 13-1 through Table 13-3 list the relationship between PHY SMBus pins to the PCH LAN SMBus pins.

**Note:** The SMBus signals (SMB\_DATA and SMB\_CLK) cannot be connected to any other devices other than the integrated MAC. Connect the SMB\_DATA and SMB\_CLK pins to the integrated MAC SML0DATA and SML0CLK pins, respectively.

### 13.1.4 PCIe and SMBus Modes

In GbE operation, PCIe is used to transmit and receive data and for MDIO status and control. The PHY automatically switches the in-band traffic between PCIe and SMBus based on the platform power state. Table 13-4 lists the operating modes of PCIe and SMBus.

The I219 GbE PHY automatically switches the in-band traffic between PCIe and SMBus based on the system power state.

**Table 13-4** PCIe and SMBus Operating Modes

System/Intel Management Engine State	PHY	
	SMBus	PCIe
S0 and PHY Power Down	Not used	Electrical Idle (EI)
S0 and Idle or Link Disconnect	Not used	EI
S0 and Link in Low Power Idle (LPI)	Not used	EI
S0 and active	Not used	Active
Sx	Active	Power down
Sx and DMoff	Active	Power down





## 13.1.5 Transitions Between PCIe and SMBus Interfaces

### 13.1.5.1 Switching from SMBus to PCIe

Communication between the integrated MAC and the PHY is done through the SMBus each time the system is in a low power state (Sx). The integrated MAC/PHY interface is needed while the Manageability Engine (ME) is still active to transfer traffic, configuration, control and status or to enable host wake up from the PHY.

Possible states for activity over the SMBus:

1. After power on (G3 to S5).
2. On system standby (Sx).

The switching from the SMBus to PCIe is done when the PE\_RST\_N signal goes high.

- Any transmit/receive packet that is not completed when PE\_RST\_N is asserted is discarded.
- Any in-band message that was sent over the SMBus and was not acknowledged is re-transmitted over PCIe.

### 13.1.5.2 Switching from PCIe to SMBus

The communication between the integrated MAC and the PHY is done through PCIe each time the platform is in active power state (S0). Switching the communication to SMBus is only needed for ME activity or to enable host wake up in low power states and is controlled by the ME.

The switching from PCIe to SMBus is done when the PE\_RST\_N signal goes low.

- Any transmit/receive packet that is not completed when PE\_RST\_N goes to 0b is discarded.
- Any in-band message that was sent over PCIe and was not acknowledged is re-transmitted over SMBus.



## 13.2 Platform LAN Design Guidelines

These sections provide recommendations for selecting components and connecting special pins. For GbE designs, the main elements are:

- The PCH chipset.
- The I219 GbE PHY.
- A magnetics module and RJ-45 connector
- A GbE region NVM (Non Volatile Memory) image
- A clock source.

**Note:** The suggested parts recommended in this section (magnetics, crystals, oscillators, etc.) are either in evaluation or have been used successfully in previous designs with good results. Intel recommends that all selected parts must be validated on each production design.

### 13.2.1 General Design Considerations for PHYs

Sound engineering practices must be followed with respect to unused inputs by terminating them with pull-up or pull-down resistors, unless otherwise specified in a datasheet, design guide or reference schematic. Pull-up or pull-down resistors must not be attached to any balls identified as “No Connect.” These devices might have special test modes that could be entered unintentionally.

#### 13.2.1.1 Clock Source

All designs require a 25-MHz clock source. The PHY uses the 25-MHz source to generate clocks up to 125 MHz and 1.25 GHz for both the PHY circuits and the PCIe interface. For optimum results with lowest cost, a 25-MHz parallel resonant crystal can be used along with the appropriate load capacitors at the XTAL\_OUT (X2) and XTAL\_IN (X1) leads. The frequency tolerance of the timing device should equal 30 ppm or better. Further detail is found in [Section 13.20](#) and [Section 13.21.15](#).

**Note:** XTAL\_OUT and XTAL\_IN are the signal names for the PHY.

There are three steps to crystal qualification:

1. Verify that the vendor’s published specifications in the component datasheet meet the required conditions for frequency, frequency tolerance, temperature, oscillation mode and load capacitance as specified in the respective datasheet.
2. Perform physical layer conformance testing and EMC (FCC and EN) testing in real systems.
3. Independently measure the component’s electrical parameters in real systems. Measure frequency at a test output to avoid test probe loading effects at the PHY. Check that the measured behavior is consistent from sample to sample and that measurements meet the published specifications. For crystals, it is also important to examine startup behavior while varying system voltage and temperature.



### 13.2.1.2 Magnetics Module

The magnetics module has a critical effect on overall IEEE and emissions conformance. The device should meet the performance required for a design with reasonable margin to allow for manufacturing variation. Carefully qualifying new magnetics modules prevents problems that might arise because of interactions with other components or the printed circuit board itself.

The steps involved in magnetics module qualification are similar to those for crystal qualification:

1. Verify that the vendor's published specifications in the component datasheet meet or exceed the required IEEE specifications.
2. Independently measure the component's electrical parameters on the test bench, checking samples from multiple lots. Check that the measured behavior is consistent from sample to sample and that measurements meet the published specifications.
3. Perform physical layer conformance testing and EMC (FCC and EN) testing in real systems. Vary temperature and voltage while performing system-level tests.

Magnetics modules for 1000BASE-T Ethernet as used by the PHY only are similar to those designed solely for 10/100 Mb/s, except that there are four differential signal pairs instead of two. Refer to the specifications section of this datasheet for specific electrical requirements that the magnetics need to meet.

While Intel does not endorse vendors or specific components, design compatibility has been verified for the connectors in [Table 13-5](#).

**Table 13-5 Integrated Magnetic Modules and Manufacturers (RJ45/USB)**

Manufacturer	Part Number	Notes
Foxconn*	JFM38U1M-7319-4F	USB2.0+USB3.0 stack, 8 core
Foxconn	JFM38U1A-21C7-4F	USB2.0 stack, 8 core
Foxconn	JFM38U1A-7126-4F	USB2.0 stack, 8 core
SpeedTech*	P25BFB4-RDW9	USB2.0 stack, 8core
SpeedTech	P35-PB4-RDW9	USB2.0 stack, 12core

**Table 13-6 Discrete Magnetics Modules: Manufacturers and Part Numbers**

Manufacturer	Part Number	Notes
Pulse*	H5120	16,51 x 9,65 x 2,08 mm, 8 core
Bothhand*	GST5009LF	15.10 x 10 x 4 mm, 8 core
Delta*	LFE9249-R-IN	15,10 x 10 x 4 mm, 8 core



**Table 13-7 Discrete RJ45**

Manufacturer	Part Number	Notes
Lotes*	AJKM0007-P001A01	Thinnest solution, 5.2 mm height
Foxconn	JM3611-NS420013-7H	Low profile, 10 mm height
Pulse	E6688-001-01-L	Low profile, 10 mm height

### 13.2.1.3 Criteria for Integrated Magnetics Electrical Qualification

Table 13-8 gives the criteria used to qualify integrated magnetics.

**Table 13-8 Integrated Magnetics Recommended Qualification Criteria**

<b>Open Circuit Inductance (OCL)</b>	w/8 mA DC bias; at 25 °C	400 µH Min
	w/8 mA DC bias; at 0 °C to 70 °C	350 µH Min
<b>Insertion Loss</b>	100 KHz through 999 KHz 1.0 MHz through 60.0 MHz 60.1 MHz through 80.0 MHz 80.1 MHz through 100.0 MHz 100.1 MHz through 125.0 MHz	1dB Max 0.6dB Max 0.8dB Max 1.0dB Max 2.4dB Max
<b>Return Loss</b>	1.0 MHz through 40.0 MHz 40.1 MHz through 100.0 MHz When reference impedance is 85 Ohms, 100 Ohms, and 115 Ohms. Note that R.L. values may vary with MDI trace lengths. The LAN magnetics may need to be measured in the platform where it will be used.	18.0 dB Min $12 - 20 * \text{LOG} (\text{Freq in MHz} / 80) \text{ dB Min}$
<b>Crosstalk Isolation Discrete Modules</b>	1.0 MHz through 29.9 MHz 30.0 MHz through 250.0 MHz 250.1 MHz through 375.0 MHz	$-50.3 + (8.8 * (\text{Freq in MHz} / 30)) \text{ dB Max}$ $-(26 - (16.8 * (\text{LOG}(\text{Freq in MHz} / 250 \text{ MHz})))) \text{ dB Max}$ -26.0 dB Max
<b>Crosstalk Isolation Integrated Modules (Proposed)</b>	1.0 MHz through 10 MHz 10.0 MHz through 100.0 MHz 100 MHz through 375.0 MHz	$-50.8 + (8.8 * (\text{Freq in MHz} / 10)) \text{ dB Max}$ $-(26 - (16.8 * (\text{LOG}(\text{Freq in MHz} / 100 \text{ MHz})))) \text{ dB Max}$ -26.0 dB Max
<b>Diff to CMR</b>	1 MHz through 29.9 MHz 30.0 MHz through 500 MHz	$-40.2 + (5.3 * ((\text{Freq in MHz} / 30))) \text{ dB Max}$ $-(22 - (14 * (\text{LOG}((\text{Freq in MHz} / 250)))) \text{ dB Max}$
<b>CM to CMR</b>	1 MHz through 270 MHz 270.1 MHz through 300 MHz 300.1 MHz through 500 MHz	$-57 + (38 * ((\text{Freq in MHz} / 270))) \text{ dB Max}$ $-17 - 2 * ((300 - (\text{Freq in MHz} / 30)) \text{ dB Max}$ -17 dB Max
<b>Hi-Voltage Isolation</b>	1500 Vrms at 50 or 60 Hz for 60 sec. or: 2250 Vdc for 60 seconds	Minimum



## 13.2.2 NVM for PHY Implementations

The LAN only supports an SPI Flash, which is connected to the PCH. Several words of the NVM are accessed automatically by the device after reset to provide pre-boot configuration data before it is accessed by host software. The remainder of the NVM space is available to software for storing the MAC address, serial numbers, and additional information.

Intel has an MS-DOS\* software utility called EEupdate that is used to program the SPI Flash images in development or production line environments. A copy of this program can be obtained through your Intel representative.

## 13.3 LAN Switch

To achieve IEEE conformance for applications that must operate both docked and undocked, a LAN switch is recommended. Note that Intel does not recommend specific switches, but those in [Table 13-8](#) have been used successfully in previous designs.

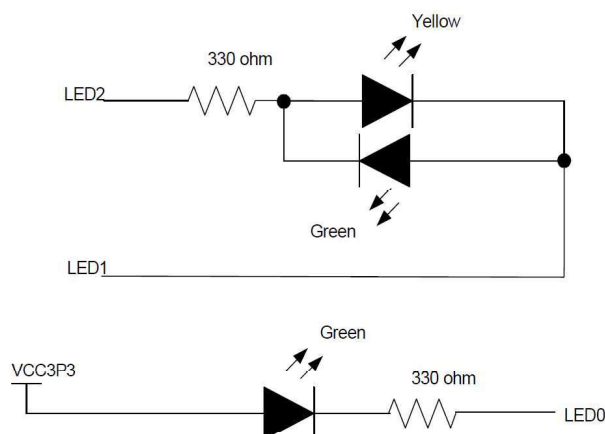
**Table 13-9 LAN Switch Manufacturers and Part Numbers**

Manufacturer	Part Number	Notes
Pericom*	PI3L720	7.0 x 3.5 x 0.75 mm. Enhanced ESD.
Pericom	PI3L500-AZ	11.0 x 5.0 x 0.75 mm. Enhanced ESD.
Texas Instruments*	TS3L500AE	11.0 x 5.0 x 0.75 mm. Enhanced ESD.



## 13.3.1 LED

The PHY has three LED outputs that can be configured via the NVM. The hardware configuration is shown in Figure 13-2.



**Figure 13-2 LED Hardware Configuration**

**Note:** Intel recommends that the LED pins only be used to drive LEDs. These pins tri-state in ULP mode and might not drive valid logic levels.

Refer to the *Intel® Ethernet Connection I219 Reference Schematic* for default LED color based on reference design.

Refer to [Section 9.0](#) of this datasheet for details regarding the programming of the LED's and the various modes. The default values for the PHY (based on the LED NVM setting--word 0x18 of the LAN region) are listed in the [Table 13-10](#).

**Table 13-10 LED Default Values**

LED	Mode	Color	Blink	Polarity
LED0	Link Up/Activity	Green	200 ms on/200 ms off	Active low
LED1	Link 1000	Yellow	No	Active low
LED2	Link 100	Green	No	Active low

### 13.3.1.1 RBIAS

RBIAS requires external resistor connection to bias the internal analog section of the device. The input is sensitive to the resistor value. Resistors of 1% tolerance must be used. Connect RBIAS through a 3.01 K $\Omega$  1% pull-down resistor to ground, then place it no more than one half inch (0.5") away from the PHY.



### **13.3.1.2 LAN Disable**

The PHY enters a power-down state when the LAN\_DISABLE\_N pin is asserted low. Exiting this mode requires setting the LAN\_DISABLE\_N pin to a logic one. Connect LAN\_DISABLE\_N to LAN\_PHY\_PWR\_CTRL GPIO12 on the PCHCougar Point-M.

## **13.3.2 Exposed Pad\* (e-Pad) Design and SMT Assembly Guide**

### **13.3.2.1 Overview**

This section provides general information about ePAD and SMT assemblies. Chip packages have exposed die pads on the bottom of each package to provide electrical interconnections with the printed circuit board. These ePADs also provide excellent thermal performance through efficient heat paths to the PCB.

Packages with ePADs are very popular due to their low cost. Note that this section provides only basic information and references in regards to the ePAD. It is recommended that each customer consult their fab and assembly house to obtain more details on how to implement the ePAD package design. Each fab and assembly house might need to tune the land pattern/stencil and create a solution that best suits their methodology and process.



## 13.3.2.2 PCB Design Requirements

To maximize both heat removal and electrical performance, a land pattern must be incorporated on the PCB within the footprint of the package corresponding to the exposed metal pad or exposed heat slug of the package as shown in the following figures. Refer to the specific product datasheet for actual dimensions.

**Note:** Due to the package size, a via-in-pad configuration must be used. Figure 13-3 and Figure 13-4 are general guidelines. See Figure 13-5 for specific via-in-pad thermal pattern recommendations.

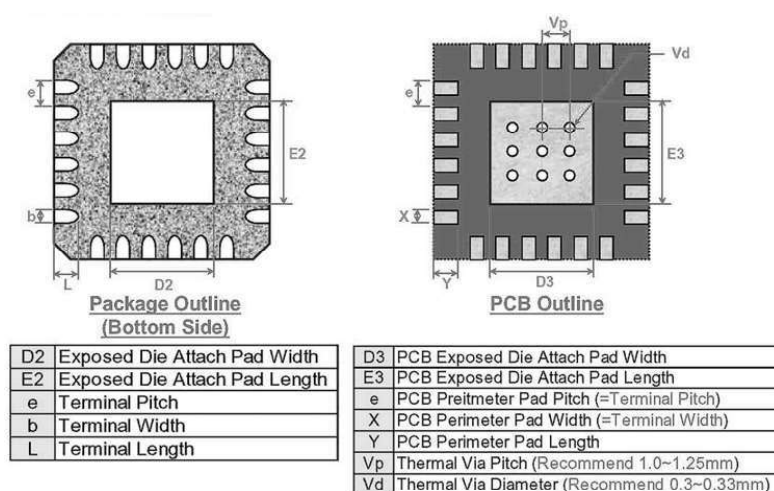


Figure 13-3 Typical ePAD Land Pattern

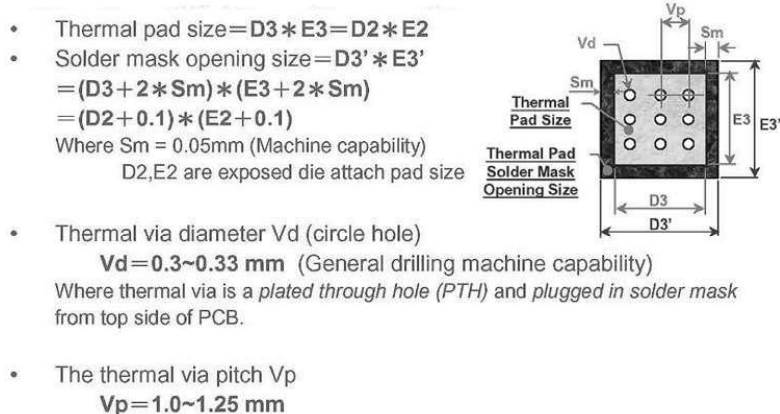


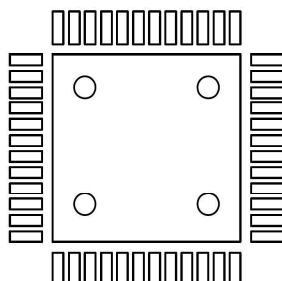
Figure 13-4 Typical Thermal Pad and Via Recommendations

**Note:** Encroached and uncapped via configurations have voids less than the maximum allowable void percentage. Uncapped via provides a path for trapped air to escape during the reflow soldering process.





**Note:** Secondary side solder bumps might be seen in an uncapped via design. This needs to be considered when placing components on the opposite side of the PHY.



**Figure 13-5 Recommended Thermal Via Patterns**

### 13.3.2.3 Board Mounting Guidelines

The following are general recommendations for mounting a QFN-48 device on the PCB. This should serve as the starting point in assembly process development and it is recommended that the process should be developed based on past experience in mounting standard, non-thermally/electrically enhanced packages.

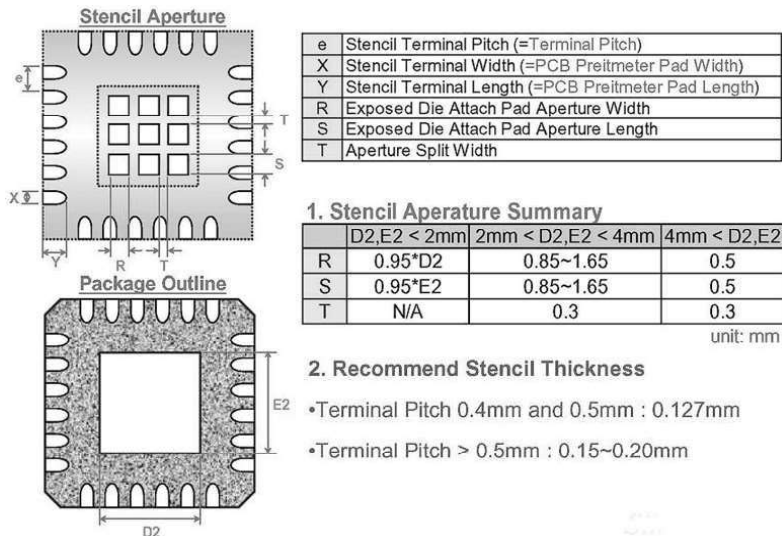
### 13.3.2.4 Stencil Design

For maximum thermal/electrical performance, it is required that the exposed pad/slug on the package be soldered to the land pattern on the PCB. This can be achieved by applying solder paste on both the pattern for lead attachment as well as on the land pattern for the exposed pad. While for standard (non-thermally/non-electrically enhanced) lead-frame based packages the stencil thickness depends on the lead pitch and package co-planarity, the package standoff must also be considered for the thermally/electrically enhanced packages to determine the stencil thickness. In this case, a stencil foil thickness in the range of 5-6 mils (or 0.127—0.152 mm) is recommended; likely or practically, a choice of either 5 mils or 6 mils. Tolerance-wise, it should not be worse than  $\pm 0.5$  mil.

**Note:** Industry specialists typically use  $\pm 0.1$  mil tolerance on stencil for its feasible precision.

The aperture openings should be the same as the solder mask openings on the land pattern. Since a large stencil opening may result in poor release, the aperture opening should be subdivided into an array of smaller openings, similar to the thermal land pattern shown in [Figure 13-6](#).

**Note:** Refer to the specific product datasheet for actual dimensions.



**Figure 13-6 Stencil Design Recommendation**

Important General Guidelines:

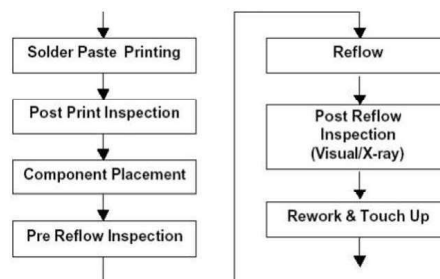
- The Stencil Aperture Openings of the e-PAD must not go outside of the exposed landing area (solder mask opening).
- The Stencil Aperture Openings of the e-PAD should be about 80% of the exposed landing area (solder mask opening).

The I219 e-PAD has D2=E2=3 mm. Therefore, the Stencil Design can only have four aperture openings for the e-PAD. This can be achieved by setting R=S=1.35 mm and T=0.3. Using this arrangement, the Aperture's/e-PAD area is 81% of the exposed landing area (solder mask opening).

**Note:** This information is intended only as general guidance. Consult with the manufacturer to confirm the final design meets requirements.

### 13.3.2.5 Assembly Process Flow

Figure 13-7 below shows the typical process flow for mounting packages to the PCB.

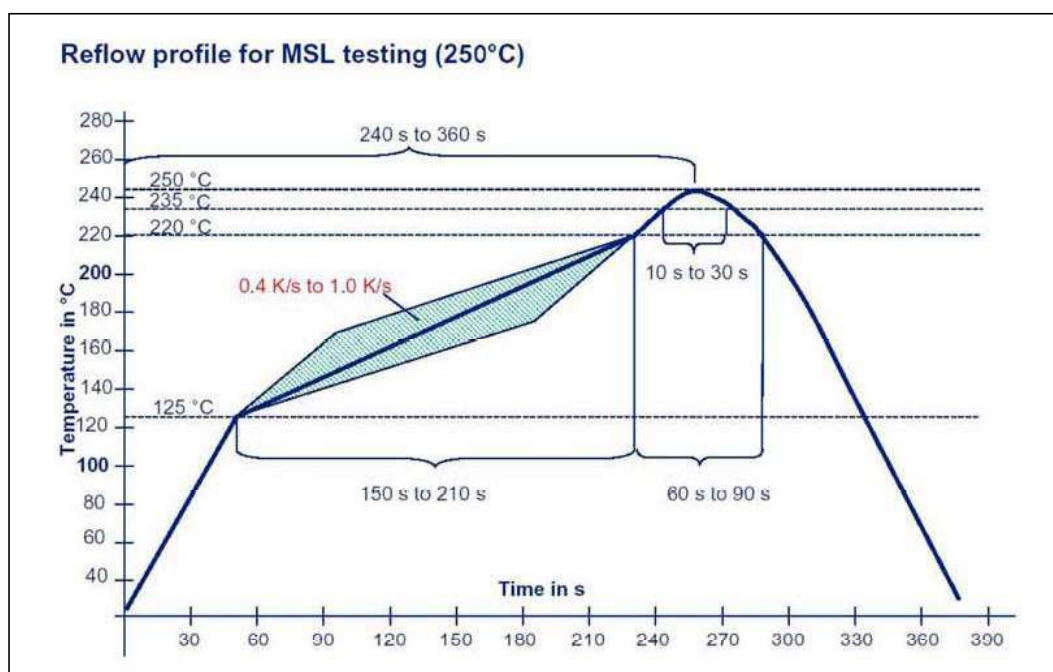


**Figure 13-7 Assembly Flow**



### 13.3.2.6 Reflow Guidelines

The typical reflow profile consists of four sections. In the preheat section, the PCB assembly should be preheated at the rate of 1 to 2 °C/sec to start the solvent evaporation and to avoid thermal shock. The assembly should then be thermally soaked for 60 to 120 seconds to remove solder paste volatiles and for activation of flux. The reflow section of the profile, the time above liquidus should be between 45 to 60 seconds with a peak temperature in the range of 245 to 250 °C, and the duration at the peak should not exceed 30 seconds. Finally, the assembly should undergo cool down in the fourth section of the profile. A typical profile band is provided in [Figure 13-8](#), in which 220 °C is referred to as an approximation of the liquidus point. The actual profile parameters depend upon the solder paste used and specific recommendations from the solder paste manufacturers should be followed.



**Notes:**

1. Preheat: 125 °C - 220 °C, 150 - 210 s at 0.4 k/s to 1.0 k/s
2. Time at T > 220 °C: 60 - 90 s
3. Peak Temperature: 245-250 °C
4. Peak time: 10 - 30 s
5. Cooling rate: ≤ 6 k/s
6. Time from 25 °C to Peak: 240 - 360 s
7. Intel recommends a maximum solder void of 50% after reflow.

**Figure 13-8 Typical Profile Band**

**Note:** Contact your Intel Field Service Representative for any designs unable to meet the recommended guidance for E-pad implementation.



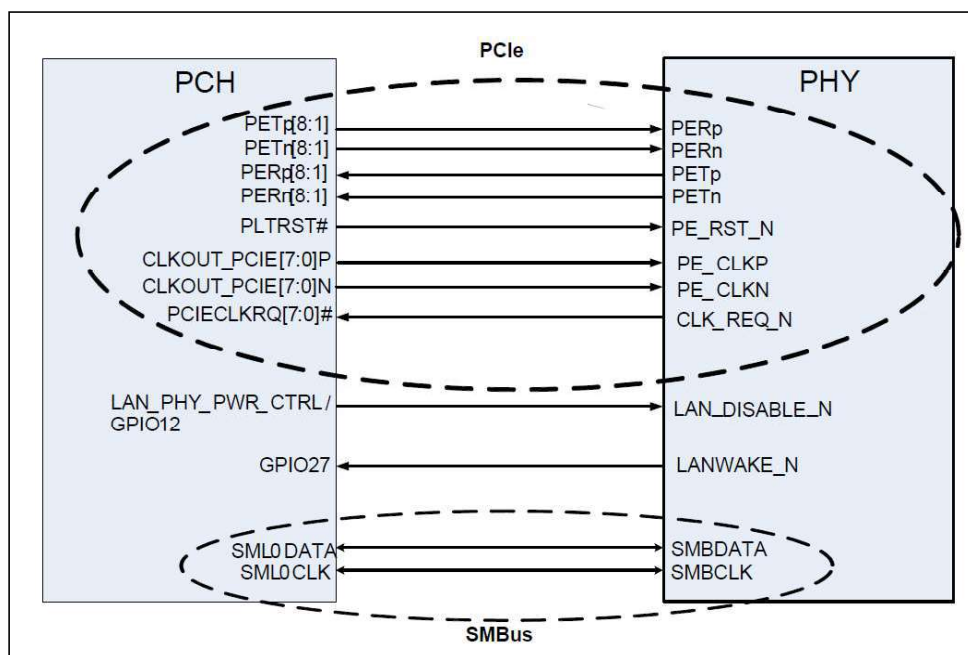
## 13.4 PCH-SMBus/PCIe LOM Design Guidelines

This section contains guidelines on how to implement a PCH/PHY single solution on a system motherboard. It should not be treated as a specification, and the system designer must ensure through simulations or other techniques that the system meets the specified timings. The following are guidelines for both PCH SMBus and PCIe interfaces. Note that PCIe is only applicable to the PHY.

The SMBus/PCIe Interface between the PCH and PHY is shown at high level in [Figure 13-9](#). For complete design details, always refer to the *Intel® Ethernet Connection I219 Reference Schematic*.

Refer to [Section 13.7](#) for PCI Express Routing Guidelines.

**Note:** Board designers MUST select the available PCIe lane based on a specific platform PCH External Design Specification (EDS). Not all PCIe lanes on a PCH are available to connect the I219 GbE PHY to the PCIe interface. For example, The SKL U/Y PCH EDS requires the I219 to only connect to PCIe ports 3, 4, 5, 9, and 10. Contact your local Intel representative for more details.



**Notes:**

1. Not all PCH PCIe ports can be used for the I219. Refer to the SkyLake/Greenlow/Purley EDS documentation for the specific ports that can be used with the I219.
2. Any CLKOUT\_PCIE and PCIECLKRQ ports can be used to connect to the I219. These can be selected using the FITC tool.
3. PETp/n, PERp/n, PE\_CLKp/n should be routed as a differential pair as indicated in the PCIe specification.
4. Refer to the I219 reference schematics and design checklists for more details.

**Figure 13-9 Single Solution Interconnect**



## 13.5 SMBus Design Considerations

No single SMBus design solution works for all platforms. Designers must consider the total bus capacitance and device capabilities when designing SMBus segments. Routing SMBus to the PCI slots makes the design process even more challenging since they add so much capacitance to the bus. This extra capacitance has a large affect on the bus time constant which in turn affects the bus rise and fall times.

Primary considerations in the design process are:

- Amount of  $V_{CC\_SUS3\_3}$  current available, that is, minimizing load of  $V_{CC\_SUS3\_3}$ .
- The pull-up resistor size for the SMBus data and clock signals is dependent on the bus load (this includes all device leakage currents). Generally the SMBus device that can sink the least amount of current is the limiting agent on how small the resistor can be. The pull-up resistor cannot be made so large that the bus time constant (Resistance X Capacitance) does not meet the SMBus rise and time specification.
- The maximum bus capacitance that a physical segment can reach is 400 pF.
- SMBus devices that can operate in STR must be powered by the  $V_{CC\_SUS3\_3}$  supply.
- It is recommended that I<sup>2</sup>C (Inter-Integrated Circuit) devices be powered by the  $V_{CC\_core}$  supply. During an SMBus transaction in which the device is sending information to the integrated MAC, the device may not release the SMBus if the integrated MAC receives an asynchronous reset.  $V_{CC\_core}$  is used to enable the BIOS to reset the device if necessary. SMBus 2.0-compliant devices have a timeout capability that makes them in-susceptible to this I<sup>2</sup>C issue, enabling flexibility in choosing a voltage supply.
- No other devices (except the integrated MAC and pull-up resistors) should be connected to the SMBus that connects to the PHY.
- **For system LAN on motherboard (LOM) designs:** The traces should be less than 70 inches for stripline and less than 100 inches for Microstrip. These numbers depend on the stackup, dielectric layer thickness, and trace width. The total capacitance on the trace and input buffers should be under 400 pF.
- **For system LAN on daughterboard designs:** Being conservative, the traces should be less than 7 inches for stripline designs and less than 10 inches for Microstrip designs. The lengths depend on the stackup, dielectric layer thickness, and trace width. Longer traces can be used as long as the total capacitance on the trace and input buffers is under 30 pF.

Note: Refer to [Section 13.1.3](#) for additional SMBus design considerations.

## 13.6 General Layout Guidelines

PHY interface signals must be carefully routed on the motherboard to meet the timing and signal quality requirements of their respective interface specifications. The following are some general guidelines that should be followed in designing a LAN solution. It is recommended that the board designer simulate the board routing to verify that the specifications are met for flight times and skews due to trace mismatch and crosstalk.



## 13.7 Layout Considerations

Critical signal traces should be kept as short as possible to decrease the likelihood of effects by high frequency noise of other signals, including noise carried on power and ground planes. This can also reduce capacitive loading.

Since the transmission line medium extends onto the printed circuit board, layout and routing of differential signal pairs must be done carefully.

Designing for GbE (1000BASE-T) operation is very similar to designing for 10/100 Mb/s. For the PHY, system level tests should be performed at all three speeds.

## 13.8 Guidelines for Component Placement

Component placement can affect signal quality, emissions, and component operating temperature. Careful component placement can:

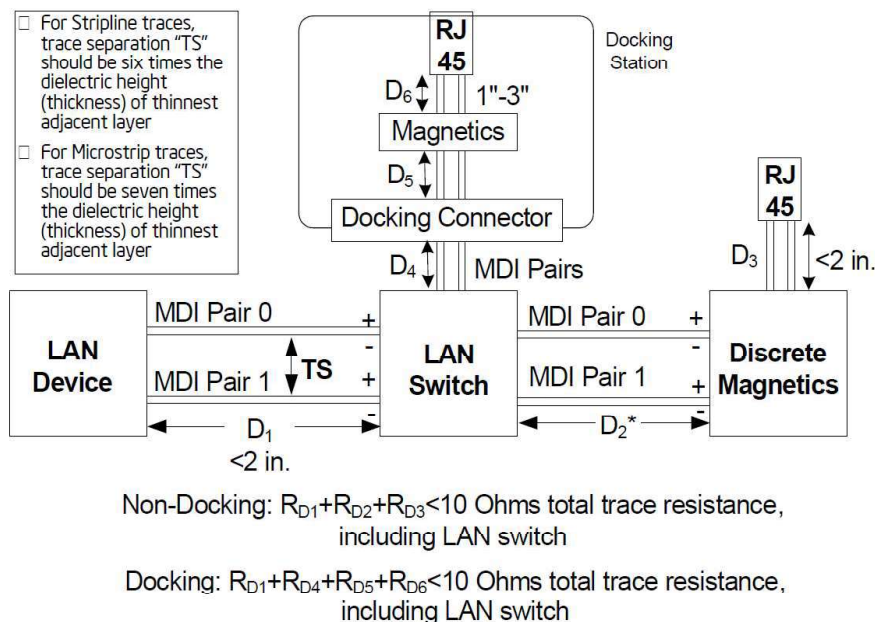
- Decrease potential problems directly related to electromagnetic interference (EMI), which could cause failure to meet applicable government test specifications. In this case, place the PHY more than one inch from the edge of the board.
- Simplify the task of routing traces. To some extent, component orientation affects the complexity of trace routing. The overall objective is to minimize turns and crossovers between traces.

### 13.8.1 PHY Placement Recommendations

Minimizing the amount of space needed for the PHY is important because other interfaces compete for physical space on a motherboard near the connector. The PHY circuits need to be as close as possible to the connector.

Figure 13-10 illustrates some basic placement distance guidelines. To simplify the diagram, it shows only two differential pairs, but the layout can be generalized for a GbE system with four analog pairs. The ideal placement for the PHY (LAN silicon) is approximately one inch behind the magnetics module.

While it is generally a good idea to minimize lengths and distances, Figure 13-10 also illustrates the need to keep the PHY away from the edge of the board and the magnetics module for best EMI performance.



\* This distance is variable and follows the general guidelines.

**Figure 13-10 LAN Device Placement: At Least One Inch from Chassis Openings or Unshielded Connectors—Mobile**

The PHY, referred to as "LAN Device" in Figure 13-10, must be at least one inch from any chassis openings. To help reduce EMI, the following recommendations should be followed:

- Minimize the length of the MDI interface. See detail in Table 13-11 on page 261.
- Place the MDI traces no closer than 0.5 inch (1.3 cm) from the board edge.
- The Intel I219 GbE PHY must be placed greater than 1" away from any hole to the outside of the chassis larger than 0.125 inches (125 mils). The larger the hole the higher the probability the EMI and ESD immunity will be negatively affected.
- The I219 should be placed greater than 250 mils from the board edge.
- If the connector or integrated magnetics module is not shielded, the I219 GbE PHY should be placed at least one inch from the magnetics (if a LAN switch is not used).
- Placing the PHY closer than one inch to unshielded magnetics or connectors increases the probability of failed EMI and common mode noise. If the LAN switch is too far away, it negatively affects IEEE return loss performance.
- The RBIAS trace length must be less than one inch.
- Place the crystal less than one inch (2.54 cm) from the PHY.



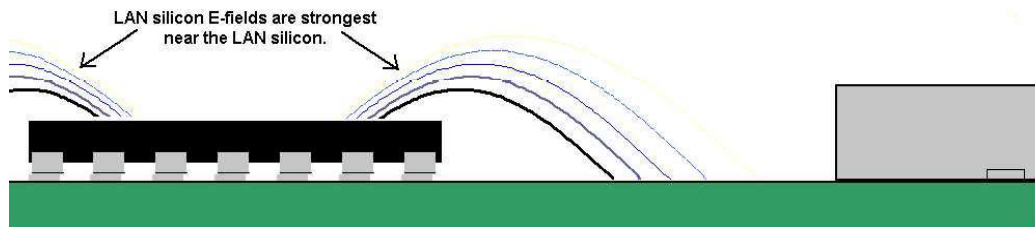


Figure 13-11 PLC Placement: At Least One Inch from I/O Backplane

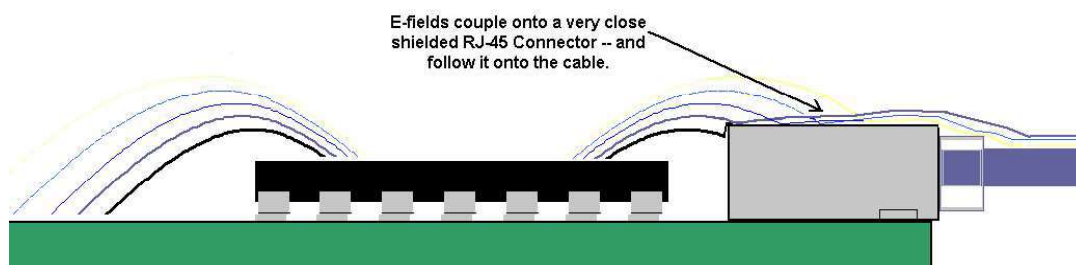


Figure 13-12 Effect of LAN Device Placed Too Close to an RJ-45 Connector or Chassis Opening

## 13.9 MDI Differential-Pair Trace Routing for LAN Design

Trace routing considerations are important to minimize the effects of crosstalk and propagation delays on sections of the board where high-speed signals exist. Signal traces should be kept as short as possible to decrease interference from other signals, including those propagated through power and ground planes.

### 13.10 Signal Trace Geometry

One of the key factors in controlling trace EMI radiation are the trace length and the ratio of trace-width to trace-height above the reference plane. To minimize trace inductance, high-speed signals and signal layers that are close to a reference or power plane should be as short and wide as practical. Ideally, the trace-width to trace-height above the ground plane ratio is between 1:1 and 3:1. To maintain trace impedance, the width of the trace should be modified when changing from one board layer to another if the two layers are not equidistant from the neighboring planes.

Each pair of signals should have a differential impedance of  $100\ \Omega \pm 15\%$ .

A set of trace length calculation tools are available from Intel to aid with MDI topology design. For access to documentation contact your Intel representative.





When performing a board layout, the automatic router feature of the CAD tool must not route the differential pairs without intervention. In most cases, the differential pairs will require manual routing.

**Note:** Measuring trace impedance for layout designs targeting 100  $\Omega$  often results in lower actual impedance due to over-etching. Designers should verify actual trace impedance and adjust the layout accordingly. If the actual impedance is consistently low, a target of 105  $\Omega$  to 110  $\Omega$  should compensate for over-etching.

It is necessary to compensate for trace-to-trace edge coupling, which can lower the differential impedance by up to 10  $\Omega$  when the traces within a pair are closer than 30 mils (edge-to-edge).

**Table 13-11 MDI Routing Summary**

Parameter	Main Route Guidelines	Breakout Guidelines <sup>1</sup>	Notes
Signal group	MDI_PLUS[0:3] MDI_MINUS[0:3]		
Microstrip/stripline uncoupled single-ended impedance specification	50 $\Omega \pm 10\%$		
Microstrip/stripline uncoupled differential impedance specification	100 $\Omega \pm 15\%$		2, 3
Microstrip nominal trace width	Design dependent	Design dependent	4
Microstrip nominal trace space	Design dependent	Design dependent	3, 5
Microstrip/stripline trace length	8 in (203 mm) maximum		6, 7
Microstrip pair-to-pair space (edge-to-edge)	$\geq 7$ times the thickness of the thinnest adjacent dielectric layer		Figure 13-13
Stripline pair-to-pair space (edge-to-edge)	$\geq 6$ times the thickness of the thinnest adjacent dielectric layer		
Microstrip bus-to-bus spacing	$\geq 7$ times the thickness of the thinnest adjacent dielectric layer		
Stripline bus-to-bus spacing	$\geq 6$ times the thickness of the thinnest adjacent dielectric layer		

**Notes:**

1. Pair-to-pair spacing  $\geq 3$  times the dielectric thickness for a maximum distance of 500 mils from the pin.
2. Board designers should ideally target 100  $\Omega \pm 15\%$ . If it's not feasible (due to board stack-up) it is recommended that board designers use a 95  $\Omega \pm 10\%$  target differential impedance for MDI with the expectation that the center of the impedance is always targeted at 95  $\Omega$ . The  $\pm 10\%$  tolerance is provided to allow for board manufacturing process variations and not lower target impedances. The minimum value of impedance cannot be lower than 85  $\Omega$ .
3. Simulation shows 80  $\Omega$  differential trace impedances degrade MDI return loss measurements by approximately 1 dB from that of 90  $\Omega$ .
4. Stripline is NOT recommended due to thinner more resistive signal layers.
5. Use a minimum of 21 mil (0.533 mm) pair-to-pair spacing for board designs that use the CRB design stack-up. Using dielectrics that are thicker than the CRB stack-up might require larger pair-to-pair spacing.
6. Mobile designs without LAN switch can range up to ~8 inches. Refer to Table 13-12 for trace length information.
7. For applications that require a longer MDI trace length of more than 8 inches (20.32 mm), it is recommended that thicker dielectric or lower Er materials be used. This permits higher differential trace impedance and wider, lower loss traces. Refer to Table 13-12 for examples of microstrip trace geometries for common circuit board materials.
8. If a LAN switch is not used, the maximum trace length is 4 inches (102 mm).



**Table 13-12 Maximum Trace Lengths Based on Trace Geometry and Board Stack-Up**

Dielectric Thickness (mils)	Dielectric Constant (DK) at 1 MHz	Width / Space/ Width (mils)	Pair-to-Pair Space (mils)	Nominal Impedance (Ohms)	Impedance Tolerance (±%)	Maximum Trace Length (inches) <sup>1</sup>
2.7	4.05	4/10/4	19	95 <sup>2</sup>	17 <sup>2</sup>	3.5
2.7	4.05	4/10/4	19	95 <sup>2</sup>	15 <sup>2</sup>	4
2.7	4.05	4/10/4	19	95	10	5
3.3	4.1	4.2/9/4.2	23	100 <sup>2</sup>	17 <sup>2</sup>	4
3.3	4.1	4.2/9/4.2	23	100	15	4.6
3.3	4.1	4.2/9/4.2	23	100	10	6
4	4.2	5/9/5	28	100 <sup>2</sup>	17 <sup>2</sup>	4.5
4	4.2	5/9/5	28	100	15	5.3
4	4.2	5/9/5	28	100	10	7

1. Longer MDI trace lengths may be achievable, but may make it more difficult to achieve IEEE conformance. Simulations have shown deviations are possible if traces are kept short. Longer traces are possible; use cost considerations and stack-up tolerance for differential pairs to determine length requirements.
2. Deviations from 100 Ω nominal and/or tolerances greater than 15% decrease the maximum length for IEEE conformance.

**Note:** Use the MDI Differential Trace Calculator to determine the maximum MDI trace length for your trace geometry and board stack-up. Contact your Intel Field Service Representative for access.

The following factors can limit the maximum MDI differential trace lengths for IEEE conformance:

- Dielectric thickness.
- Dielectric constant.
- Nominal differential trace impedance.
- Trace impedance tolerance.
- Copper trace losses.
- Additional devices, such as switches, in the MDI path may impact IEEE conformance.

Board geometry should also be factored in when setting trace length.

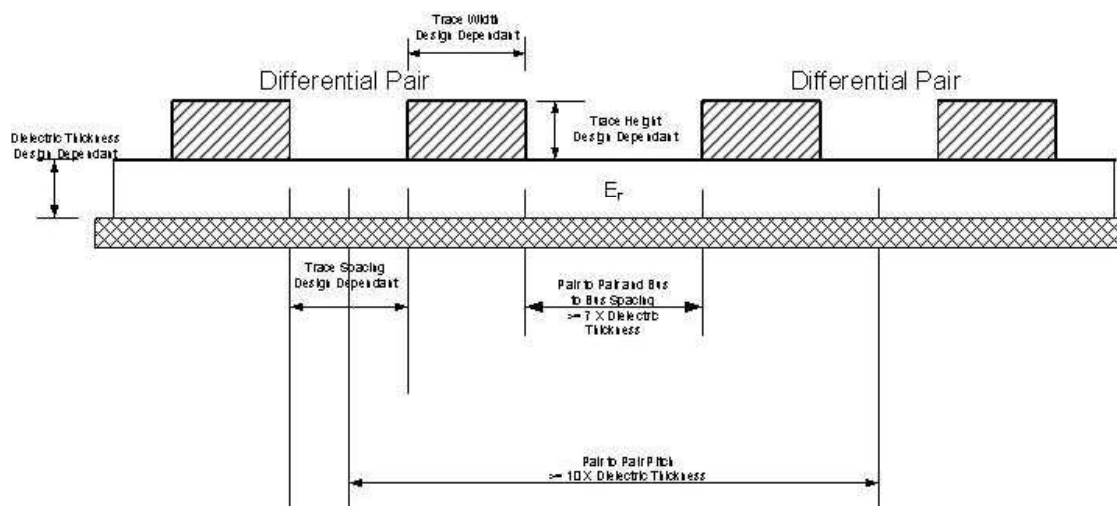


Figure 13-13 MDI Trace Geometry

## 13.11 Trace Length and Symmetry

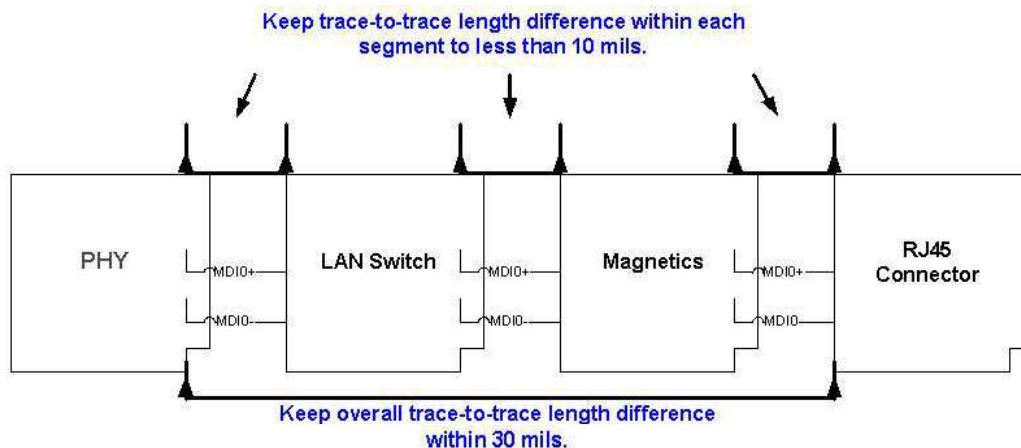
The differential traces should be equal in total length to within 10 mils (0.254 mm) per segment within each pair and as symmetrical as possible. Asymmetrical and unequal length traces in the differential pairs contribute to common mode noise. If a choice has to be made between matching lengths and fixing symmetry, more emphasis should be placed on fixing symmetry. Common mode noise can degrade the receive circuit's performance and contribute to radiated emissions.

The intra-pair length matching on the pairs must be within 10 mils on a segment by segment basis. An MDI segment is defined as any trace within the same layer. For example, transitioning from one layer to another through a via is considered as two separate MDI segments.

The end to end total trace lengths within each differential pair must match as shown in Figure 13-13. The end to end trace length is defined as the total MDI length from one component to another regardless of layer transitions.

The pair to pair length matching is not as critical as the intra-pair length matching but it should be within 2 inches.

When using Microstrip, the MDI traces should be at least 7x the thinnest adjacent dielectric away from the edge of an adjacent reference plane. When using stripline, the MDI traces should be at least 6x the thinnest adjacent dielectric away from the edge of an adjacent reference plane.



**Figure 13-14 MDI Differential Trace Geometry**

**Note:** Similar topology applies to MDI routing from the I219 to the dock RJ45 connector.

## 13.12 Impedance Discontinuities

Impedance discontinuities cause unwanted signal reflections. Vias (signal through holes) and other transmission line irregularities should be minimized. If vias must be used, a reasonable budget is four or less per differential trace. Unused pads and stub traces should also be avoided.

## 13.13 Reducing Circuit Inductance

Traces should be routed over a continuous reference plane with no interruptions. If there are vacant areas on a reference or power plane, the signal conductors should not cross the vacant area. This causes impedance mismatches and associated radiated noise levels.

## 13.14 Signal Isolation

Also, keep the MDI traces away from the edge of an adjacent reference plane by a distance that is at least 7x the thickness of the thinnest adjacent dielectric layer (7x when using Microstrip; 6x when using stripline). If digital signals on other board layers cannot be separated by a ground plane, they should be routed perpendicular to the differential pairs. If there is another LAN controller on the board, the differential pairs from that circuit must be kept away.



Other rules to follow for signal isolation include:

- Separate and group signals by function on separate layers if possible. If possible, maintain at least a gap of 30 mils between all differential pairs (Ethernet) and other nets, but group associated differential pairs together.
- Physically group together all components associated with one clock trace to reduce trace length and radiation.
- Isolate I/O signals from high-speed signals to minimize crosstalk, which can increase EMI emission and susceptibility to EMI from other signals.
- Avoid routing high-speed LAN traces near other high-frequency signals associated with a video controller, cache controller, processor, switching power supplies, or other similar devices.

## 13.15 Power and Ground Planes

Good grounding requires minimizing inductance levels in the interconnections and keeping ground returns short, signal loop areas small, and power inputs bypassed to signal return. This will significantly reduce EMI radiation.

The following guidelines help reduce circuit inductance in both backplanes and motherboards:

- Route traces over a continuous plane with no interruptions. Do not route over a split power or ground plane. If there are vacant areas on a ground or power plane, avoid routing signals over the vacant area. This will increase inductance and EMI radiation levels.
- All ground vias should be connected to every ground plane; and every power via, to all power planes at equal potential. This helps reduce circuit inductance.
- Physically locate grounds between a signal path and its return. This will minimize the loop area.
- Split the ground plane beneath a magnetics module. The RJ-45 connector side of the transformer module should have chassis ground beneath it.

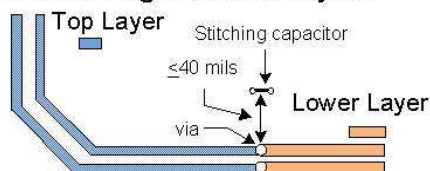
**Caution:** DO NOT do this if the RJ-45 connector has integrated USB.

**Note:** All impedance-controlled signals should be routed in reference to a solid plane. If there are plane splits on a reference layer and the signal traces cross those splits, stitching capacitors should be used within 40 mils of where the crossing occurs. See [Figure 13-15](#).

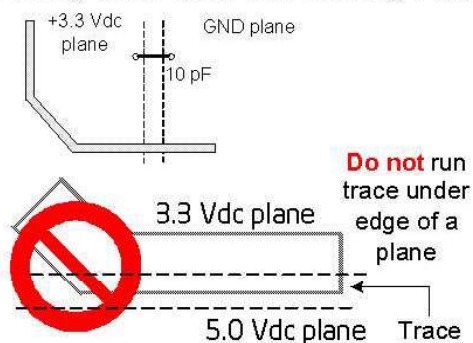
If signals transition from one reference layer to another reference layer then stitching capacitors or connecting vias should be used based on the following:

- If the transition is from power-referenced layer to a ground-referenced layer or from one voltage-power referenced layer to a different voltage-power referenced layer, then stitching capacitors should be used within 40 mils of the transition.
- If the transition is from one ground-referenced layer to another ground-referenced layer or is from a power-referenced layer to the same net power-referenced layer, then connecting vias should be used within 40 mils of the transition.

### Transitioning Reference Layers



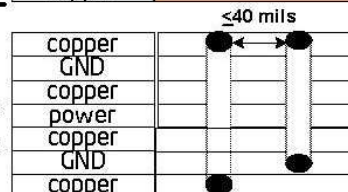
### Crossing Plane Splits-Use Stitching Capacitors



Distance from stitching capacitor to any via is ≤40 mils



Connection Vias  
GND to GND



Connection Vias  
PWR to same PWR

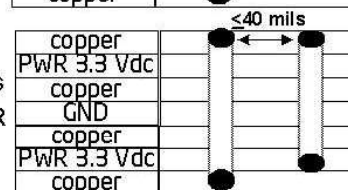


Figure 13-15 Trace Transitioning Layers and Crossing Plane Splits

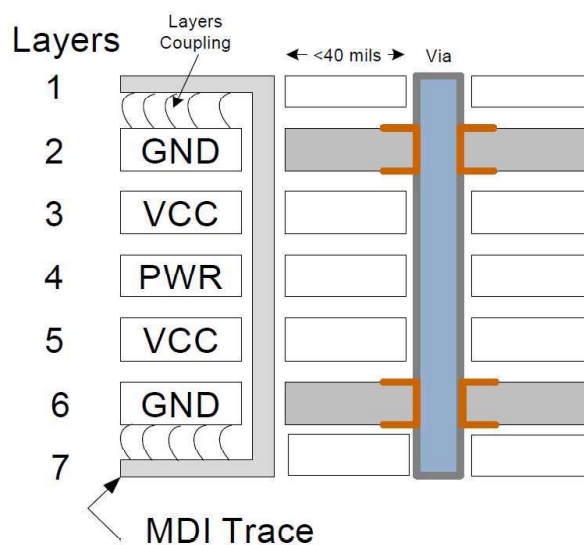
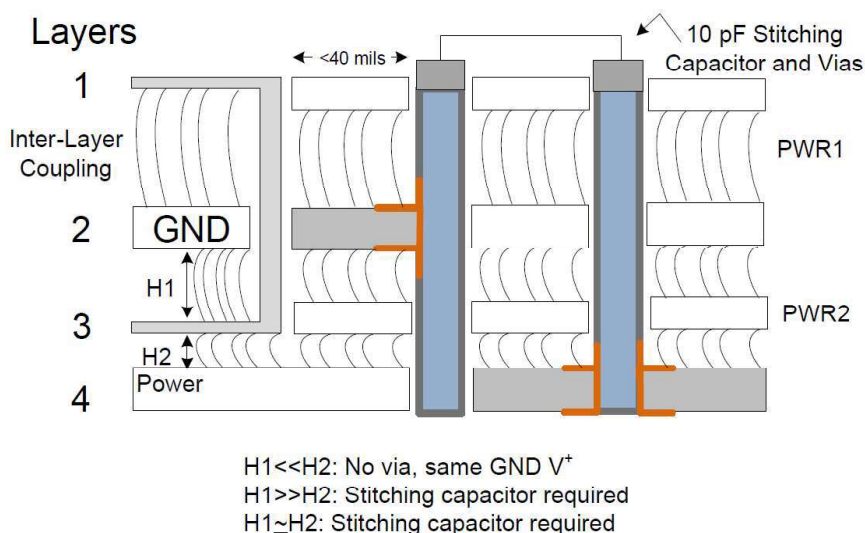


Figure 13-16 Via Connecting GND to GND



### Figure 13-17 Stitching Capacitor Between Vias Connecting GND to GND

## 13.16 Traces for Decoupling Capacitors

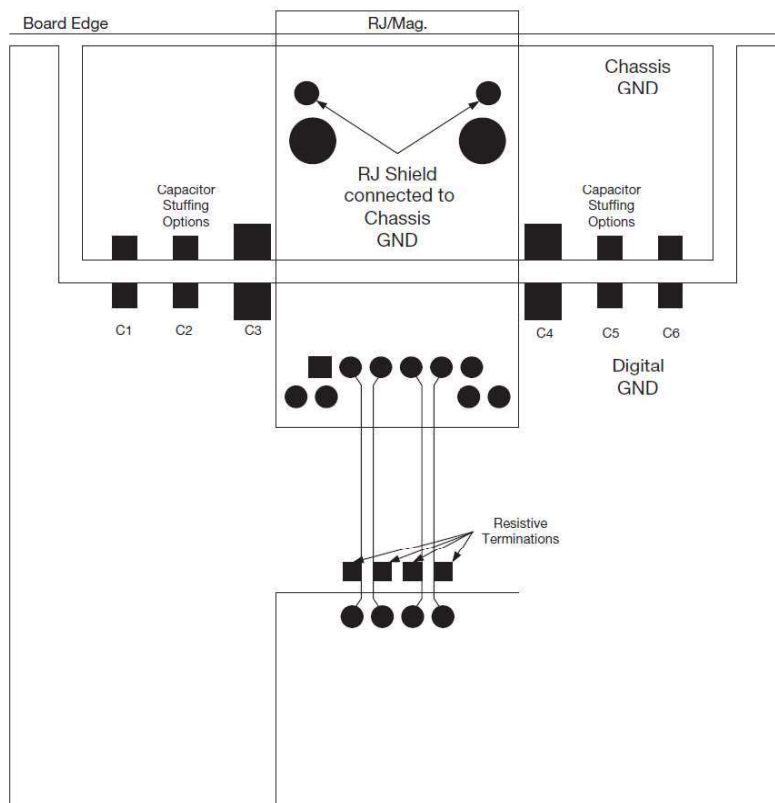
Traces between decoupling and I/O filter capacitors should be as short and wide as practical. Long and thin traces are more inductive and reduce the intended effect of decoupling capacitors. Also, for similar reasons, traces to I/O signals and signal terminations should be as short as possible. Vias to the decoupling capacitors should be sufficiently large in diameter to decrease series inductance. Refer to the Power Delivery section for the PHY in regards to actual placement requirements of the capacitors.

### 13.17 Ground Planes Under a Magnetics Module

The magnetics module chassis or output ground (secondary side of transformer) should be separated from the digital or input ground (primary side) by a physical separation of 100 mils minimum. Splitting the ground planes beneath the transformer minimizes noise coupling between the primary and secondary sides of the transformer and between the adjacent coils in the magnetics. This arrangement also improves the common mode choke functionality of magnetics module.

**Caution:** DO NOT do this if the RJ-45 connector has integrated USB.

Figure 13-18 shows the preferred method for implementing a ground split under an integrated magnetics module/RJ-45 connector.



**Figure 13-18 Ideal Ground Split Implementation**

**Table 13-13 Capacitor Stuffing Option Recommended Values**

Capacitors	Value
C3, C4	4.7 $\mu$ F or 10 $\mu$ F
C1, C2, C5, C6	470 pF to 0.1 $\mu$ F

The placement of C1 through C6 may also differ for each board design (in other words, not all of the capacitors may need to be populated). Also, the capacitors may not be needed on both sides of the magnetics module.

**Note:** If using an integrated magnetics module without USB, provide a separate chassis ground "island" to ground around the RJ-45 connector. The split in the ground plane should be at least 20 mils wide.

Some integrated magnetics modules/RJ-45 connectors have recently incorporated the USB into the device. For this type of magnetics module, a chassis ground moat may not be feasible due to the digital ground required for the USB pins and their placement relative to the magnetics pins. Thus, a continuous digital ground without any moats or splits must be used. [Figure 13-19](#) provides an example of this.



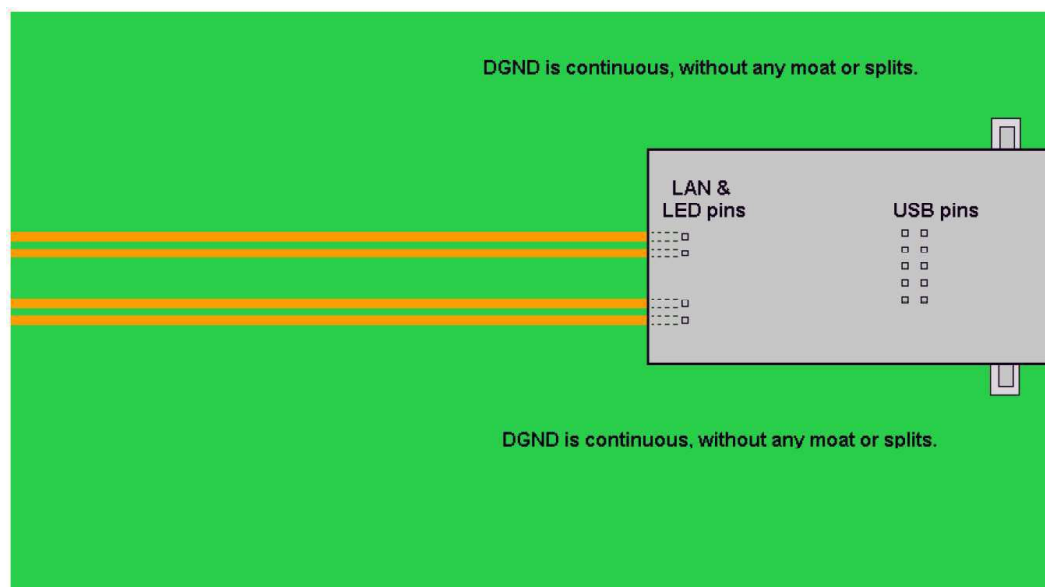


Figure 13-19 Ground Layout with USB

## 13.18 Light Emitting Diodes

The device has three high-current outputs to directly drive LEDs for link, activity and speed indication. Since LEDs are likely to be integral to a magnetics module, take care to route the LED traces away from potential sources of EMI noise. In some cases, it may be desirable to attach filter capacitors.

LAN LED traces should be placed at least 6x (side by side separation) the dielectric height from sources of noise (ex: signaling traces) and susceptible signal traces (ex: reset signals) on the same or adjacent layers.

LAN LED traces should be placed at least 7x (broadside coupling) the dielectric height from sources of noise (ex: signaling traces) and susceptible signal traces (ex: reset signals) on the same or adjacent layers.

## 13.19 Considerations for Layout

The PHY MDI routing using microstrip requires a differential impedance of  $100\ \Omega \pm 15\%$ . A 35-mil (0.889 mm) separation is required between pairs. The 35-mil separation can be reduced for 24 mils (0.61 mm) in breakout routing. All MDI traces must be referenced to ground.



## 13.20 Frequency Control Device Design Considerations

This section provides information regarding frequency control devices, including crystals and oscillators, for use with all Intel Ethernet controllers. Several suitable frequency control devices are available; none of which present any unusual challenges in selection. The concepts documented within this section are applicable to other data communication circuits, including the PHY.

The PHY contains amplifiers that form the basis for feedback oscillators when they are used with the specific external components. These oscillator circuits, which are both economical and reliable, are described in more detail in [Section 13.21.3](#).

The chosen frequency control device vendor should be consulted early in the design cycle. Crystal and oscillator manufacturers familiar with networking equipment clock requirements may provide assistance in selecting an optimum, low-cost solution.

Several types of third-party frequency reference components are currently available. Descriptions of each type follow in subsequent sections. They are also listed in order of preference.

## 13.21 Crystals and Oscillators

Clock sources should not be placed near I/O ports or board edges. Radiation from these devices may be coupled onto the I/O ports or out of the system chassis. Crystals should also be kept away from the Ethernet magnetics module to prevent interference.

Crystal and load capacitors should be placed on the printed circuit boards as close to the PHY as possible, which is within 1.0 inch. Traces from XTAL\_IN (X1) and XTAL\_OUT (X2) should be routed as symmetrically as possible. Do not route X1 and X2 as a differential trace. Doing so increases jitter and degrades LAN performance.

- The crystal trace lengths should be less than 1 inch.
- The crystal load capacitors should be placed less than 1" from the crystal.
- The clock lines must be at least 5 times the height of the thinnest adjacent dielectric layer away from other digital traces (especially reset signals), I/O ports, board edge, transformers and differential pairs.
- The clock lines must not cross any plane cuts on adjacent power or ground reference layers unless there are decoupling capacitors or connecting vias near the transition.
- The clock lines should not cross or run in parallel (within 3x the dielectric thickness of the closest dielectric layer) with any trace (100 MHz signal or higher) on an adjacent layer.

### 13.21.1 Quartz Crystal

Quartz crystals are generally considered to be the mainstay of frequency control components due to their low cost and ease of implementation. They are available from numerous vendors in many package types and with various specification options.



## 13.21.2 Fixed Crystal Oscillator

A packaged fixed crystal oscillator comprises of an inverter, a quartz crystal, and passive components conveniently packaged together. The device renders a strong, consistent square wave output. Oscillators used with microprocessors are supplied in many configurations and tolerances.

Crystal oscillators should be restricted for use in special situations, such as shared clocking among devices or multiple controllers. Since clock routing can be difficult to accomplish, it is preferable to provide a separate crystal for each device.

**Note:** Contact your Intel Field Service Representative to obtain the most current device documentation prior to implementing this solution.

## 13.21.3 Crystal Selection Parameters

All crystals used with Intel Ethernet controllers are described as “AT-cut,” which refers to the angle at which the unit is sliced with respect to the long axis of the quartz stone.

Table 13-14 lists crystals which have been used successfully in past designs. (No particular product is recommended.)

**Table 13-14 Crystal Manufacturers and Part Numbers**

Manufacturer	Part Number	Notes
Epson*	Q22FA1280021400	2.0 x 1.6 x 0.5mm Small part. Loading capacitors = 10 pF.
TXC Corporation, USA*	8Y25000010	2.0 x 1.6 x 0.5mm Small part. Loading capacitors = 10 pF.
TXC Corporation, USA	7M25020011	3.2 x 2.5 x 0.7 mm
TXC Corporation, USA	9C25000008	HC-49S type, SMD (low profile 3 mm)
NDK America, Inc.*	EXS00A-CH00387	3.2 x 2.5 x 0.8mm
NDK America, Inc.	41CD25.0F1303018	HC-49S type, SMD

The datasheet for the PHY lists the crystal electrical parameters and provides suggested values for typical designs. Designers should refer to criteria outlined in their respective PHY datasheet. The parameters are described in the following subsections.

## 13.21.4 Vibrational Mode

Crystals in the frequency range referenced above are available in both fundamental and third overtone. Unless there is a special need for third overtone, fundamental mode crystals should be used.



## 13.21.5 Nominal Frequency

Intel Ethernet controllers use a crystal frequency of 25.000 MHz. The 25 MHz input is used to generate a 125-MHz transmit clock for 100BASE-TX and 1000BASE-TX operation, and 10-MHz and 20-MHz transmit clocks, for 10BASE-T operation.

## 13.21.6 Frequency Tolerance

The frequency tolerance for an Ethernet Platform LAN Connect device is dictated by the IEEE 802.3 specification as  $\pm 50$  parts per million (ppm). This measurement is referenced to a standard temperature of 25 °C. Intel recommends a frequency tolerance of  $\pm 30$  ppm to ensure for any frequency variance contributed by the PCB.

## 13.21.7 Temperature Stability and Environmental Requirements

Temperature stability is a standard measure of how the oscillation frequency varies over the full operational temperature range (and beyond). Several optional temperature ranges are currently available, including -40 °C to +85 °C for industrial environments. Some vendors separate operating temperatures from temperature stability. Manufacturers may also list temperature stability as 50 ppm in their data sheets.

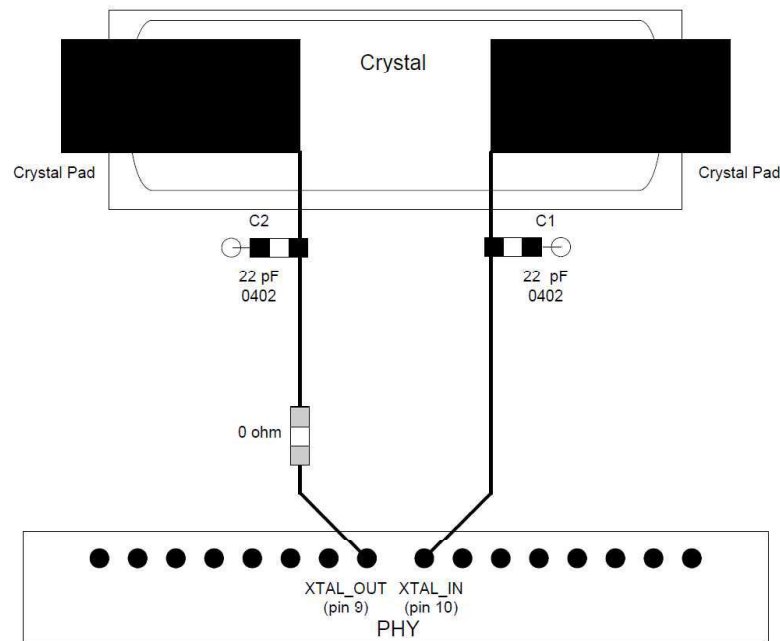
**Note:** Crystals also carry other specifications for storage temperature, shock resistance, and reflow solder conditions. Crystal vendors should be consulted early in the design cycle to discuss its application and environmental requirements.

## 13.21.8 Calibration Mode

The terms “series-resonant” and “parallel-resonant” are often used to describe crystal oscillator circuits. Specifying parallel mode is critical to determining how the crystal frequency is calibrated at the factory.

A crystal specified and tested as series resonant oscillates without problem in a parallel-resonant circuit, but the frequency is higher than nominal by several hundred parts per million. The purpose of adding load capacitors to a crystal oscillator circuit is to establish resonance at a frequency higher than the crystal’s inherent series resonant frequency.

Figure 13-20 illustrates a simplified schematic of the internal oscillator circuit. Pin X1 and X2 refers to XTAL\_IN and XTAL\_OUT in the Ethernet device, respectively. The crystal and the capacitors form a feedback element for the internal inverting amplifier. This combination is called parallel-resonant, because it has positive reactance at the selected frequency. In other words, the crystal behaves like an inductor in a parallel LC circuit. Oscillators with piezoelectric feedback elements are also known as “Pierce” oscillators.



**Figure 13-20 Thermal Oscillator Circuit**

## 13.21.9 Load Capacitance

The formula for crystal load capacitance is as follows:

$$C_L = \frac{(C1 \cdot C2)}{(C1 + C2)} + C_{\text{stray}}$$

where  $C1 = C2 = 22 \text{ pF}$  (as suggested in most Intel reference designs), and  $C_{\text{stray}}$  = allowance for additional capacitance in pads, traces and the chip carrier within the Ethernet device package and  $C_{\text{damp}}$ .

## 13.21.10 Shunt Capacitance

The shunt capacitance parameter is relatively unimportant compared to load capacitance. Shunt capacitance represents the effect of the crystal's mechanical holder and contacts. The shunt capacitance should be a maximum of 6 pF.



## 13.21.11 Equivalent Series Resistance

Equivalent Series Resistance (ESR) is the real component of the crystal's impedance at the calibration frequency, which the inverting amplifier's loop gain must overcome. ESR varies inversely with frequency for a given crystal family. The lower the ESR, the faster the crystal starts up. Crystals with an ESR value of 50  $\Omega$  or better should be used.

## 13.21.12 Drive Level

Drive level refers to power dissipation in use. The allowable drive level for a Surface Mounted Technology (SMT) crystal is less than its through-hole counterpart. This is due to the fact that surface mount crystals are typically made from narrow, rectangular AT strips, rather than circular AT quartz blanks.

When selecting a crystal, board designers must ensure that the crystal specification meets at least the drive level specified. For example, if the crystal drive level specification states that the drive level is 200  $\mu\text{W}$  maximum, then the crystal drive level must be at least 200  $\mu\text{W}$ . So, a 500  $\mu\text{W}$  crystal is sufficient, but a 100  $\mu\text{W}$  crystal is not.

## 13.21.13 Aging

Aging is a permanent change in frequency (and resistance) occurring over time. This parameter is most important in its first year because new crystals age faster than old crystals. Crystals with a maximum value of  $\pm 5$  ppm per year aging should be used.

## 13.21.14 Reference Crystal

The normal tolerances of the discrete crystal components can contribute to small frequency offsets with respect to the target center frequency. To minimize the risk of tolerance-caused frequency offsets causing a small percentage of production line units to be outside of the acceptable frequency range, it is important to account for those shifts while empirically determining the proper values for the discrete loading capacitors, C1 and C2.

Even with a perfect support circuit, most crystals will oscillate slightly higher or lower than the exact center of the target frequency. Therefore, frequency measurements, which determine the correct value for C1 and C2, should be performed with an ideal reference crystal. When the capacitive load is exactly equal to the crystal's load rating, an ideal reference crystal will be perfectly centered at the desired target frequency.



### 13.21.14.1 Reference Crystal Selection

There are several methods available for choosing the appropriate reference crystal:

- If a Saunders and Associates (S&A) crystal network analyzer is available, then discrete crystal components can be tested until one is found with zero or nearly zero ppm deviation (with the appropriate capacitive load). A crystal with zero or near zero ppm deviation will be a good reference crystal to use in subsequent frequency tests to determine the best values for C1 and C2.
- If a crystal analyzer is not available, then the selection of a reference crystal can be done by measuring a statistically valid sample population of crystals, which has units from multiple lots and approved vendors. The crystal, which has an oscillation frequency closest to the center of the distribution, should be the reference crystal used during testing to determine the best values for C1 and C2.
- It may also be possible to ask the approved crystal vendors or manufacturers to provide a reference crystal with zero or nearly zero deviation from the specified frequency when it has the specified  $C_{Load}$  capacitance.

When choosing a crystal, customers must keep in mind that to comply with IEEE specifications for 10/100 Mb/s operation and 10/100/1000 Mb/s operation if applicable, the transmitter reference frequency must be precise within  $\pm 50$  ppm. Intel recommends customers use a transmitter reference frequency that is accurate to within  $\pm 30$  ppm to account for variations in crystal accuracy due to crystal manufacturing tolerance.

### 13.21.14.2 Circuit Board

Since the dielectric layers of the circuit board are allowed some reasonable variation in thickness, the stray capacitance from the printed board (to the crystal circuit) will also vary. If the thickness tolerance for the outer layers of dielectric are controlled within  $\pm 15\%$  of nominal, then the circuit board should not cause more than  $\pm 2$  pF variation to the stray capacitance at the crystal. When tuning crystal frequency, it is recommended that at least three circuit boards are tested for frequency. These boards should be from different production lots of bare circuit boards.

Alternatively, a larger sample population of circuit boards can be used. A larger population will increase the probability of obtaining the full range of possible variations in dielectric thickness and the full range of variation in stray capacitance.

Next, the exact same crystal and discrete load capacitors (C1 and C2) must be soldered onto each board, and the LAN reference frequency should be measured on each circuit board.

The circuit board, which has a LAN reference frequency closest to the center of the frequency distribution, should be used while performing the frequency measurements to select the appropriate value for C1 and C2.

### 13.21.14.3 Temperature Changes

Temperature changes can cause the crystal frequency to shift. Therefore, frequency measurements should be done in the final system chassis across the system's rated operating temperature range.



## 13.21.15 Oscillator Support

The PHY clock input circuit is optimized for use with an external crystal. However, an oscillator can also be used in place of the crystal with the proper design considerations (refer to the PHY Datasheet for detailed clock oscillator specifications):

- The clock oscillator has an internal voltage regulator to isolate it from the external noise of other circuits to minimize jitter. If an external clock is used, this imposes a maximum input clock amplitude. For example, if a 3.3 V DC oscillator is used, its output signal should be attenuated to a maximum value with a resistive divider circuit.
- The input capacitance introduced by the PHY (approximately 11 to 13 pF) is greater than the capacitance specified by a typical oscillator (approximately 15 pF).
- The input clock jitter from the oscillator can impact the PHY clock and its performance.

**Note:** The power consumption of additional circuitry equals about 1.5 mW.

Table 13-15 lists oscillators that can be used with the PHY. Note that no particular oscillator is recommended.

**Table 13-15 Oscillator Manufacturers and Part Numbers**

Manufacturer	Part Number	Notes
TXC Corporation - USA	8W25080004	2.5 x 2.0 x 0.8mm.
TXC Corporation - USA	7X25080001	3.2 x 2.5 x 1.0 mm.

## 13.21.16 Oscillator Placement and Layout Recommendations

Oscillator clock sources should not be placed near I/O ports or board edges. Radiation from these devices can be coupled into the I/O ports and radiate beyond the system chassis. Oscillators should also be kept away from the Ethernet magnetics module to prevent interference.

The oscillator must have its own decoupling capacitors and they must be placed within 0.25 inches. If a power trace is used (not power plane), the trace from the capacitor to the oscillator must not exceed 0.25 inches in length. The decoupling capacitors help to improve the oscillator stability. The oscillator clock trace should be less than two inches from the PHY. If it is greater than 2 inches, then verify the signal quality, jitter, and clock frequency measurements at the PHY.

The clock lines should also target  $5\ \Omega \pm 15\%$  and should have  $10\ \Omega$  series back termination placed close to the series oscillator. To help reduce EMI, the clock lines must be a distance of at least five times the height of the thinnest adjacent dielectric layer away from other digital traces (especially reset signals), I/O ports, the board edge, transformers and differential pairs.

The clock lines must not cross any plane cuts on adjacent power or ground reference layers unless there are decoupling capacitors or connecting vias near the transition. The clock lines should not cross or run in parallel with any trace (100 MHz signal or higher) on an adjacent layer.





There should be a ferrite bead within 250 mils of the oscillator power pin and there must be a 1  $\mu$ F or greater capacitor within 250 mils of the oscillator, connected to the power trace between the oscillator input and ferrite bead. With a ferrite bead on the power trace for the oscillator, there should be a power pour (or fat trace) to supply power to the oscillator.

**Note:** For the latest PHY schematic connection recommendations, refer to the *Intel® I219 GbE PHY Reference Schematic* and the *Intel® I219 GbE PHY Schematic and Layout Checklist*, available through your Intel representative.

## 13.22 Troubleshooting Common Physical Layout Issues

The following lists common physical layer design and layout mistakes in LAN on Motherboard (LOM) designs.

1. Lack of symmetry between the two traces within a differential pair. Asymmetry can create common-mode noise and distort the waveforms. For each component and via that one trace encounters, the other trace should encounter the same component or a via at the same distance from the Ethernet silicon.
2. Unequal length of the two traces within a differential pair. Inequalities create common-mode noise and will distort the transmit or receive waveforms.
3. Excessive distance between the Ethernet silicon and the magnetics. Long traces on FR4 fiberglass epoxy substrate will attenuate the analog signals. In addition, any impedance mismatch in the traces will be aggravated if they are longer than the four-inch guideline.
4. Routing any other trace parallel to and close to one of the differential traces. Crosstalk getting onto the receive channel will cause degraded long cable BER. Crosstalk getting onto the transmit channel can cause excessive EMI emissions and can cause poor transmit BER on long cables. At a minimum, for stripline other signals should be kept at least 6x the height of the thinnest adjacent dielectric layer. For microstrip it is 7x. The only possible exceptions are in the vicinities where the traces enter or exit the magnetics, the RJ-45 connector, and the Ethernet silicon.
5. Using a low-quality magnetics module.
6. Reusing an out-of-date physical layer schematic in a Ethernet silicon design. The terminations and decoupling can be different from one PHY to another.
7. Incorrect differential trace impedances. It is important to have about a 100- $\Omega$  impedance between the two traces within a differential pair. This becomes even more important as the differential traces become longer. To calculate differential impedance, many impedance calculators only multiply the single-ended impedance by two. This does not take into account edge-to-edge capacitive coupling between the two traces. When the two traces within a differential pair are kept close to each other, the edge coupling can lower the effective differential impedance by 5  $\Omega$  to 20  $\Omega$ . Short traces will have fewer problems if the differential impedance is slightly off target.

## 13.23 Power Delivery

The I219 requires a 3.3 V power rail and a 0.93 V (Core) power rail. The internal 3.3 V power rail is brought out for decoupling. [Figure 2-2](#) shows a typical power delivery configuration that can be



implemented. However, power delivery can be customized based on a specific OEM. In general planes should be used to deliver 3.3 Vdc and the Core voltage. Not using planes can cause resistive voltage drop and/or inductive voltage drop (due to transient or static currents). Some of the symptoms of these voltage drops can include higher EMI, radiated immunity, radiated emissions, IEEE conformance issues, and register corruption.

Decoupling capacitors (0.1  $\mu$ F and smaller) should be placed within 250 mils of the LAN device. They also should be distributed around the PHY and some should be in close proximity to the power pins.

The bulk capacitors (1.0  $\mu$ F or greater) should be placed within 1 inch if using a trace (50 mils wide or wider) or within 1.5 inches if using a plane.

The Core power rail for the I219 uses the integrated SVR (iSVR). When laying out the circuit the inductor must be placed within 0.5" of the input pin to the PHY and connected with a trace wider than or equal to 20 mil wide. (See the reference schematic for further details regarding the Core power rail.)

While Intel does not endorse vendors or specific components, design compatibility has been verified for the connectors in [Table 13-16](#).

**Table 13-16 Inductors and Manufacturers**

Manufacturer	Part Number	Notes
Taiyo Yuden*	NRS2012T-4R7MGJ	2.0 x 2.0 x 1.2 mm
TDK*	VLS2012ET-4R7M	2.0 x 2.0 x 1.2 mm
muRata*	LQH32PN4R7NN0	3.2 x 2.5 x 1.55 mm
muRata	LQH32CN4R7M53	3.2 x 2.5 x 1.55 mm

**Note:** For latest PHY schematic connection recommendations, refer to the *Intel® I219 GbE PHY Reference Schematic* or contact your Intel Field Service Representative.

## 13.24 I219 Power Sequencing

The Intel® Ethernet Controller I219 does not require any power sequencing between the 3.3 V and Core power rails. See the reference schematic for details.